State and Timing Modules for Agilent Technologies Logic Analysis Systems

Product Overview

Your design team faces a difficult challenge: Deliver quality products to the marketplace faster than your competitors. Meeting that challenge depends on your ability to debug and characterize hardware, design and test firmware and software, and perform system integration.

Hardware and software engineers need a common, scalable system for testing and debugging digital systems. Agilent Technologies offers a variety of measurement modules for logic analysis systems to make it easy for you to select the right solution today then expand as your needs evolve without relearning or reinvesting in the platform.

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Choose the Logic Analyzer and Measurement Modules that Best Fit Your Application

State/Timing Modules	General-purpose hardware debug	8/16 Bit processor debug	32/64 Bit processor debug or channel intensive systems	High-speed bus analysis	Timing margin analysis or characterize setup/hold	Deep trace capture with timing or state analysis	High-speed computer debug	Analysis of data intensive systems and performance
16710A	√	√						
16711A	√	√						
16712A	√	√						
16557D		√	√			√		
16715A			√			√	√	
16716A	√	√	√		√		√	
16717A			√	√	√	√	√	
16718A			√	√	√	√	√	√
16719A			√	√	√	√	√	√
16517/18A				√	√			

A variety of measurement modules allow you to select the optimum combination of performance, features, and price to meet your specific needs now and in the future.

Agilent Technologies
Innovating the HP Way

Key Specifications* and Characteristics

Model	NEW 16715A	NEW 16716A	NEW 16717A, 16718A, 16719A
Maximum state clock*	167 MHz	167 MHz	333 MHz [1]
Maximum timing sample rate (full/half channel)	Conventional: 333/667 MHz	2 GHz Timing Zoom Conventional: 333/667 MHz	2 GHz Timing Zoom Conventional: 333/667 MHz
Channels/module	68	68	68
Maximum channels on a single time base and trigger	340	340	340
Maximum channels in a system	680	680	680
Memory depth (full/half channel)	2/4M [2]	512K/1M [2]	16717A 2/4M [2] 16718A 8/16M [2] 16719A 32/64M [2]
Trigger resources	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [4] Global Counters: 2 Flags: 8	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [4] Global Counters: 2 Flags: 8	Patterns: 16 Ranges: 15 Edge & Glitch: 2 Timers: (2 per module) -1 Occurrence Counter: [4] Global Counters: 2 Flags: 8
Maximum trigger sequence levels	16	16	16
Maximum trigger sequence speed	167 MHz	167 MHz	333 MHz
Trigger sequence level branching	4-way arbitrary IF/THEN/ELSE branching	4-way arbitrary IF/THEN/ELSE branching	4-way arbitrary IF/THEN/ELSE branching
Number of state clocks/qualifiers	4	4	4
Setup/hold time*	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel [3]		
Threshold range	TTL, ECL, user-definable ±6.0 V adjustable in 10-mV increments		

[1] State speeds greater than 167 MHz require a trade-off in features. Refer to "Supplemental Specifications and Characteristics" on page 20 for more information.
[2] Memory depth doubles in half-channel timing mode only.
[3] Minimum setup/hold time specified for a single clock, single edge acquisition. Multi-clock, multi-edge setup/hold window add 0.5 ns.
[4] There is one occurrence counter per trigger sequence level.

Key Specifications* and Characteristics (cont'd)

Model	16710A, 16711A, 16712A	16557D		16517A/18A
		1-4 Modules	5 Modules	
Maximum state clock*	100 MHz	140 MHz	100 MHz	1 GHz synchronous state [1]
Maximum timing sample rate (full/half channel)	Conventional: 250/500 MHz Transitional: 125 MHz	Conventional: 250/500 MHz		Conventional: 2/4 GHz
Channels/module	102	68		16
Maximum channel count on a single time base and trigger	204	272	340	80
Maximum channels in a system	1020	680		160
Memory depth (full/half channel)	16710A 8/16K [2] 16711A 32/64K [2] 16712A 128/256K [2]	2/4M [2]		64/128K [2]
Trigger resources	Patterns: 10 Ranges: 2 Edge & Glitch: 2 Timers: 2	Patterns: 10 Ranges: 2 Edge & Glitch: 2 Timers: 2		Patterns: 4 Edge & Glitch: 2 Timers:[3]
Trigger sequence levels	State mode: 12 Timing mode: 10	State mode: 12 Timing mode: 10		State mode: 4 Timing mode: 4
Maximum trigger sequence speed	125 MHz	140 MHz		500 MHz [1]
Trigger sequence level branching	Dedicated next state or single arbitrary branching			
Number of state clocks/qualifiers	6	4		1[4]
Setup/hold time*	4.0 ns window adjustable from 4.0/0 ns to 0/4.0 ns in 500 ps increments [6] per 34 channels	3.0 ns window adjustable from 3.0/0 ns to -0.5/3.5 ns in 500 ps increments [6] per 34 channels		700 ps window adjustable from 350/350 ps adjustable in 50 ps increments [5] per 8 channels
Threshold range	TTL, ECL, user-definable ±6.0 V adjustable in 50-mV increments			TTL, ECL, user-definable ± 5 V adjustable in 10-mV increments

[1] The Agilent Technologies 16517A, 16518A have a maximum trigger sequencer speed of 500 MHz. Triggering on data at speeds faster than 500 MHz requires the data to be valid for a minimum of 2.25 ns.
[2] Memory depth doubles in half-channel timing mode only.
[3] There is one timer or counter per sequence level, which is restarted upon entry into each level.
[4] Requires a periodic clock from 20 MHz to 1 GHz. Clock edge is selectable as positive or negative.
[5] The setup and hold across pods is 750/750 ps without manual adjustment, 350/350 ps with manual adjustment.
[6] Minimum setup/hold time specified for single-clock, single-edge acquisition. Single-clock, multi-edge setup/hold add 0.5 ns. Multi-clock, multi-edge setup/hold window add 1.0 ns.

How to Evaluate Your Logic Analysis Needs

State Speed

State analysis uses a signal from your system under test to determine when to sample. Since state analysis samples are synchronous with the system under test, it will provide you with a view of how your system is executing. You can use state analysis to capture bus cycles from a microprocessor or I/O bus and convert the data into processor mnemonics or bus transactions using an Agilent Technologies inverse assembler.

Select a state acquisition system that provides the speed you need without breaking your budget. Remember that a processor will specify an internal core frequency that is normally 2X-5X the speed of the external bus.

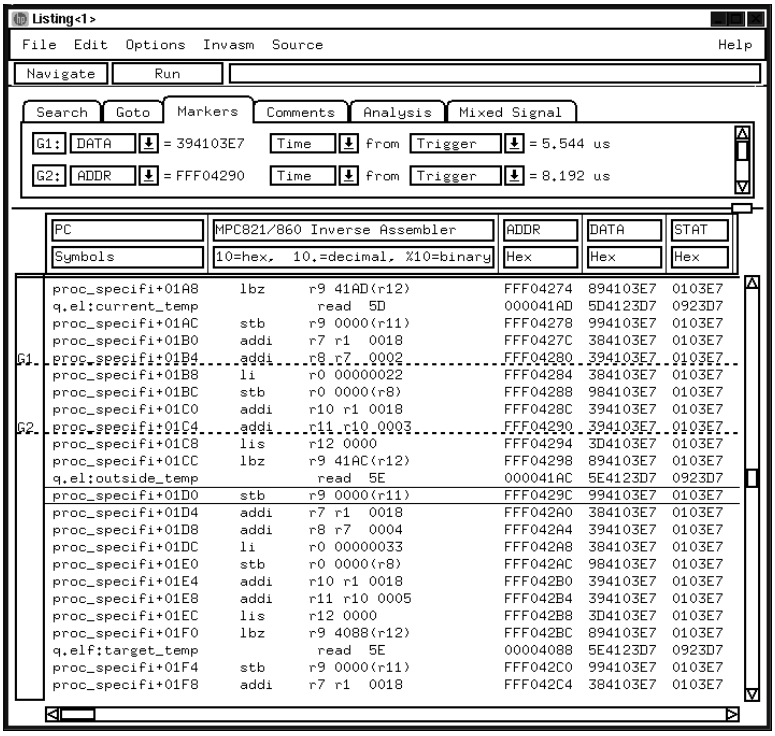


Figure 1. State analysis allows you to track real-time system execution problems.

Setup/Hold

Logic analyzers are like any logic circuitry in that they require time for the data at the inputs to become valid (setup time), and time to capture the data (hold time). As your target frequencies increase, the ability of your logic analyzer to capture accurate data is limited by its setup and hold. A lengthy setup and hold can make the difference between capturing valid data or data in transition.

Your device under test will ensure data is valid on the bus for a defined length of time. This is known as the data valid window. Your target's data valid window must be large enough to meet the setup/hold specifications of the logic analyzer. The data valid window of most devices is generally less than half of the clock period. Don't be fooled by "typical" setup and hold specifications. To ensure the capture of valid data, the maximum setup/hold time for your logic analyzer must fit within your target's data valid window.

Inaccurate measurements can also result when the logic analyzer's setup/hold window cannot be positioned within the target's data valid window. An adjustable setup/hold with fine position resolution provides unparalleled measurement accuracy at high frequencies.

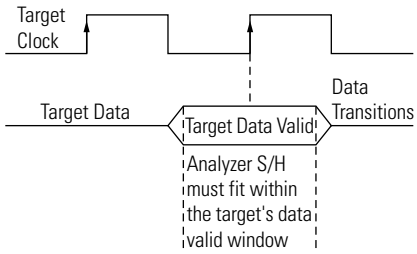


Figure 2. Make sure your logic analyzer captures accurate data.

Timing Resolution
Timing analysis uses the logic analyzer's internal clock to determine when to sample. Since timing analysis samples asynchronously to the system under test, you should consider what accuracy you will need to verify your system. Accuracy is made up of two elements: sample speed and channel-to-channel skew. Remember to evaluate both of these elements and be careful of logic analyzers that have a fast sample speed with a large channel-to-channel skew.

Transitional Timing
If your system has bursts of activity followed by times with little activity, you can use transitional timing to capture a longer trace. In transitional timing, the analyzer samples data at regular intervals, but only stores the data when there is a transition on one of the signals.

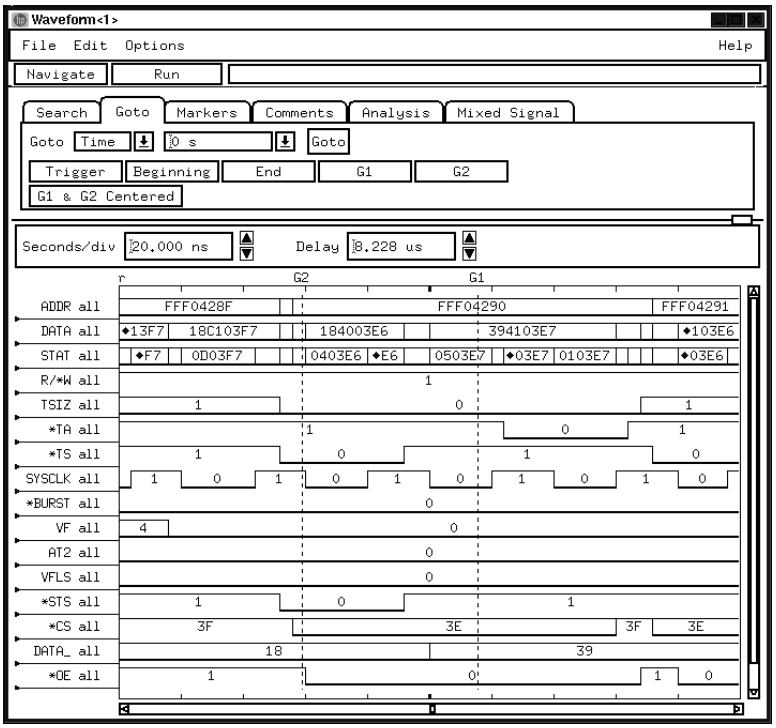


Figure 3. Evaluate time relationships between signals with timing analysis.

Channel Count
Determine the number of signals you want to analyze on your system under test. You will need this number of channels in your logic analyzer. Even if you have enough channels to view all the signals in your system today, you should consider logic analysis systems that allow you to add more channels for your future application needs.

Memory
Deep memory is an invaluable resource when you trigger on a problem symptom that is far removed from its cause. This is common in complex systems that have a significant amount of hardware/software interaction. Software engineers will also appreciate the ability to capture deep traces to view code execution.

Much of your debug time is spent analyzing captured data. When using deep memory,consider a logic analysis system with the performance you need to help you quickly sift through measurement results.

Triggering
The logic analyzer memory system is similar to a circular buffer. When the acquisition is started, the analyzer continuously acquires data samples and stores them in memory. When memory becomes full, it simply wraps around and stores each new sample in the place of the sample that has been in memory the longest.
This process will continue until the logic analyzer finds the trigger point. The logic analyzer trigger stops the acquisition at the point you specify and provides a view into the system under test. The primary responsibility of the trigger is to stop the acquisition, but it can also be used to control the selective storage of data. Consider a logic analyzer with the trigger resources you need to quickly set up your measurements.

Improve your Productivity with an Intuitive User Interface

You may not use your logic analyzer every day, therefore Agilent Technologies has made the user interface easy to understand. Now you can spend more time making measurements and less time setting up the logic analyzer.

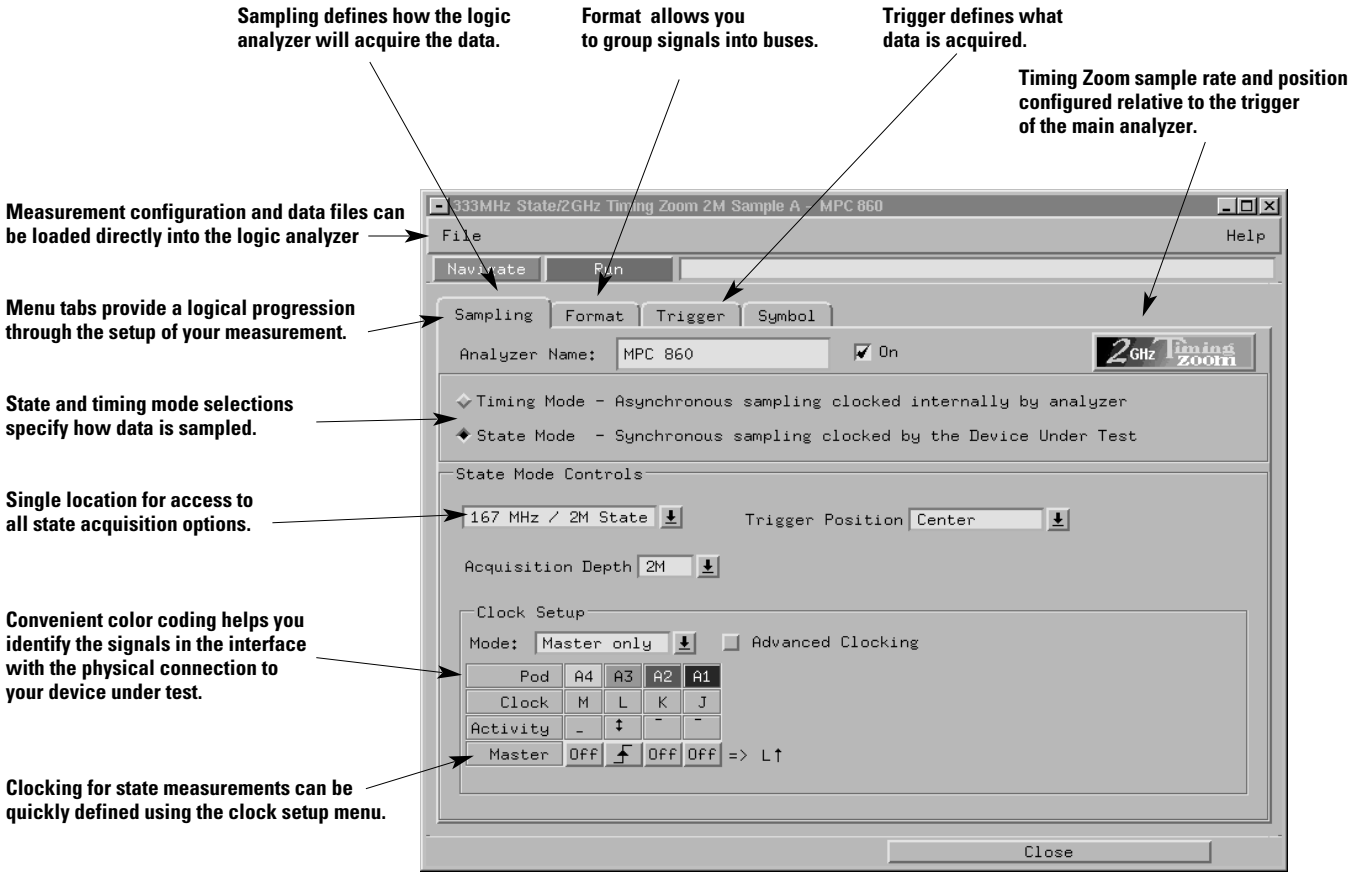


Figure 4. Setting up your logic analyzer has never been this easy to understand.

Agilent Technologies' New VisiTrigger™ Technology Allows You To Quickly Locate Your Most Elusive Problems

VisiTrigger™ technology available in the 16715A, 16716A, 16717A, 16718A, and 16719A family of modules is a breakthrough in logic analysis usability. It combines increased trigger functionality with a user interface that is easy to understand and use. Now with VisiTrigger™, capturing complex events is as simple as point-and-click to choose the trigger function and fill-in-the-blank to customize it to your specific task.

View up-to-date information on the current state of the timers, counters, flags, and the trigger sequence level.

Save and recall up to ten of your custom trigger setups without loading a new configuration file.

Your most commonly used triggers are just a mouse click away with the built-in trigger functions. VisiTrigger's graphical representation shows you how the trigger condition will be defined. You can use trigger functions as building blocks to easily customize a trigger for your specific task.

Sequence levels allow you to develop a sequence of analyzer instructions to specify a trigger point or to qualify data and store only the information that interests you. Each step in the sequence contains an "IF/THEN/ELSE" structure that can evaluate up to four logic events. Each event can specify a combination of actions such as: store sample, increment counters, reset timers, trigger, or go to another step in the sequence level.

Ranges provide a way to monitor program and data accesses within a specified area in memory.

Global counters can count events such as the number of times a function executes or accesses an I/O port.

Timers can be set up to evaluate when one event happens too late or too soon with respect to another event.

In timing mode, edge terms let you trigger on a rising edge, falling edge, either edge, or a glitch.

Patterns and their logical combinations let you identify which states to store, when to branch and when to trigger.

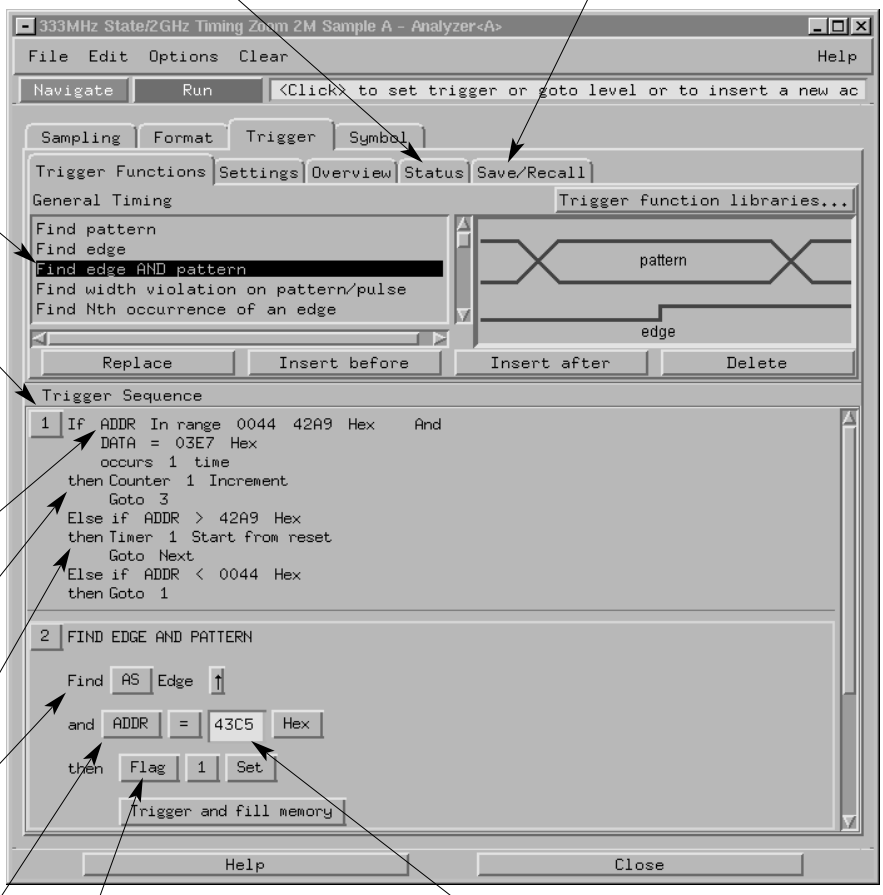


Figure 5. Set up your trigger in terms of the measurements you want to make.

Flags can be set, cleared and evaluated by any 16715/16/17/18/19A module in the frame. This allows you to set up a trigger that is dependent on activity from more than one bus in the system.

Values can be easily entered directly into the trigger description.

2 GHz Timing Zoom Provides High-Speed Timing Analysis Across All Channels, All the Time

The 16716A, 16717A, 16718A, and 16719A state/timing modules provide a breakthrough in logic analysis performance by allowing you to acquire up to 2 GHz timing and high-speed state data simultaneously through the same connection to your device under test.

2 GHz Timing Zoom provides superior flexibility in high-speed data capture with a variable sample rate from 250 MHz to 2 GHz, 16K memory depth, and variable placement of Timing Zoom data around the trigger point.

With Timing Zoom's 500 ps resolution, you can now use the wide channel count of a logic analyzer to improve the efficiency of your hardware characterization process.

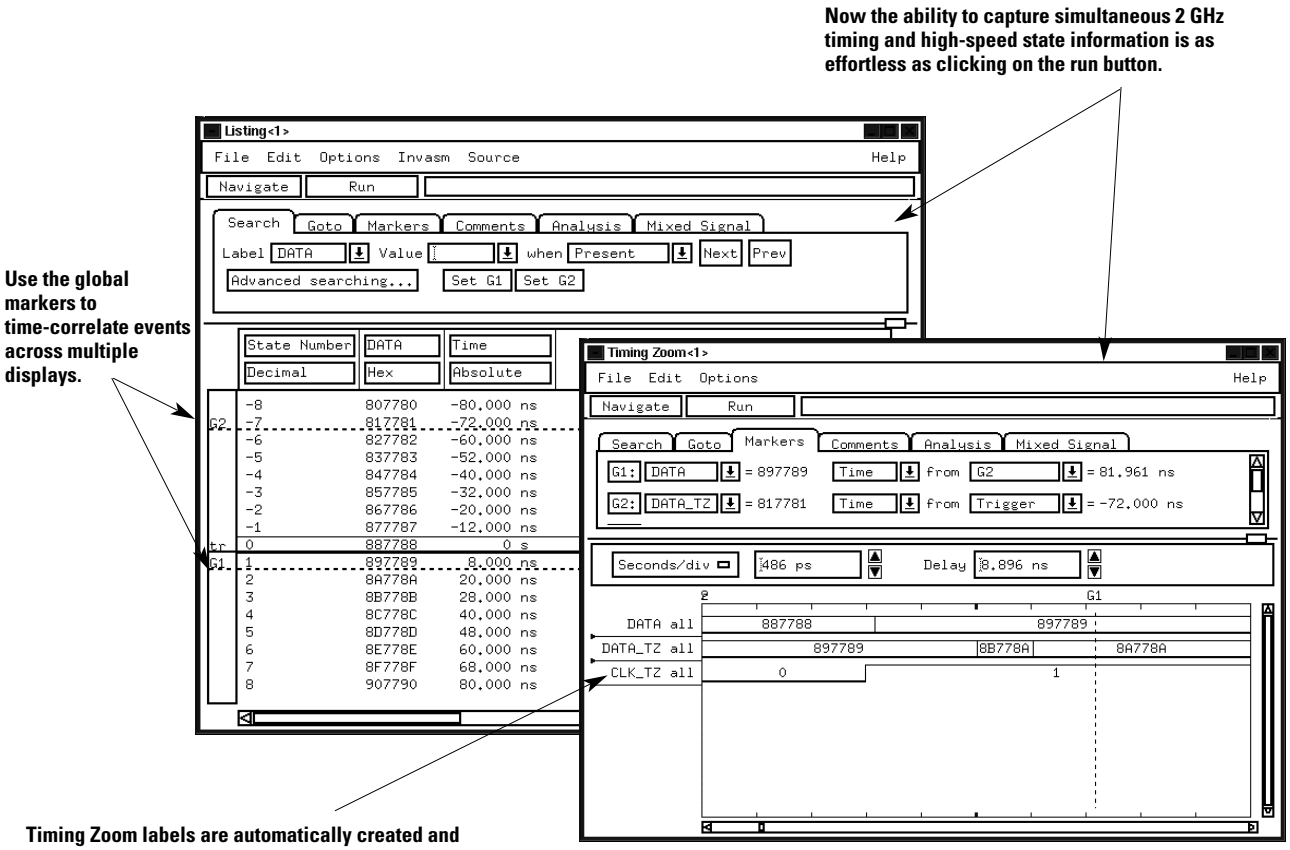


Figure 6. Verifying critical edge timing in your system just got easier with Agilent Technologies' 2 GHz Timing Zoom technology.

Insure the Capture of Difficult to Reproduce System Problems

Memory depth can be an invaluable resource when you are trying to link the symptom of a problem to its root cause. Extensive acquisition memory allows you to view long periods of code execution, capture deep traces of timing information, optimize your system for peak performance, or validate your ASIC design against EDA simulations.

Usable Deep Memory

The key to deep memory is system performance. The 16718A and 16719A modules include the following innovative hardware enhancements to improve the performance and usability of large data sets:

- **Hardware Accelerated Search**
  Even if the pattern you specify is not found in the entire 32M trace, the search takes only a few seconds.

- **Fast Waveform Draw**
  The entire 32M waveform can be drawn on screen in a matter of seconds, then you can draw a box around an area and quickly zoom in to explore the details.

- **Fast Binary Out**
  The ability for you to quickly remove data from the logic analyzer has also been optimized.

- **Constant Feedback with Cancel**
  You are provided with feedback on percent to completion of the operation, and you have the option to cancel it at any time.

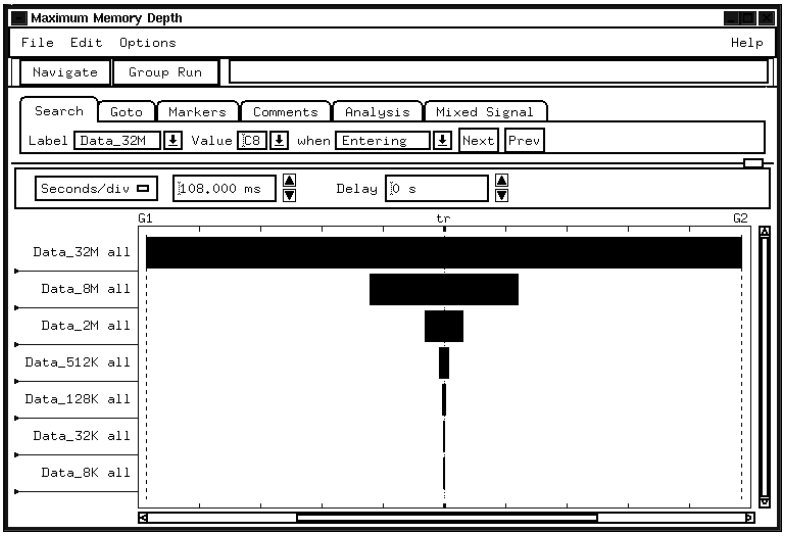


Figure 7. Agilent Technologies offers a variety of memory depths to fit your price/performance needs

Note: Some Agilent Technologies tools are limited to a maximum memory depth of 2M because they create multiple large data records. These tools are: Compare, B4601B serial analysis tool set, B4605B tool development kit.

Deep memory traces create large data files when you save the acquired data. For this reason, option #008 has been added to the 16700A-Series mainframes to provide an 18 GB external hard drive. This option is recommended when you use the 16718A and 16719A modules.

Why is Probing Important?

Your debugging tools perform three important tasks: probing your target system, acquiring data, and analyzing data. Data acquisition and analysis tools are only as effective as the physical interface to your target system. Use the following criteria to see how your probing measures up.

Immunity to Noise

EMF noise is everywhere, and it can corrupt your data. Active attenuator probing can be particularly susceptible to noise effects. Agilent Technologies designs probing solutions with high immunity to transient noise.

Impedance

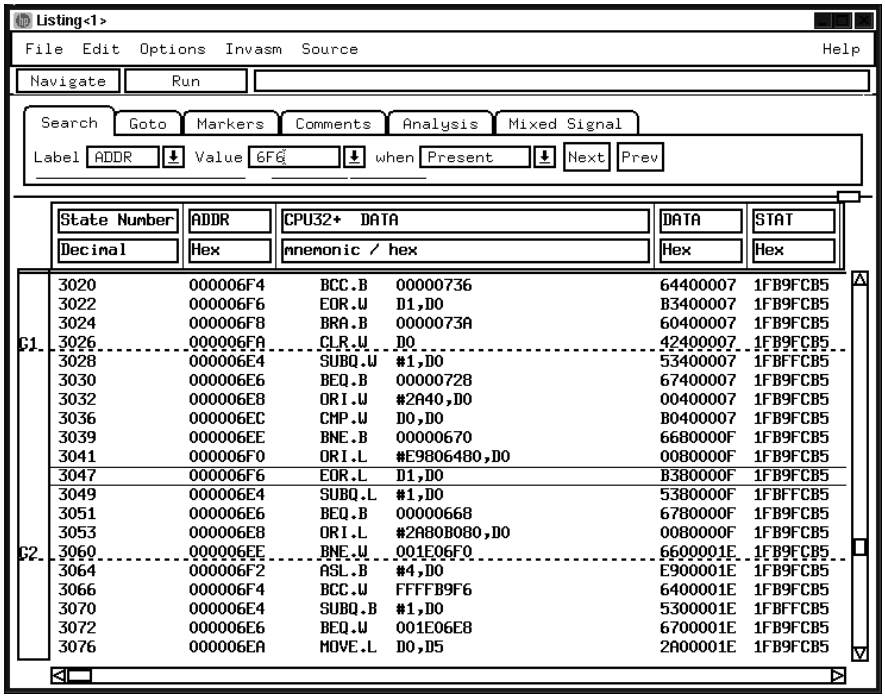
High input impedance will minimize the effect of probing on your circuit. Although many probes are acceptable for lower frequencies, probing effects become very significant at higher frequencies.

Ruggedness

A flimsy probe will give you unintended open circuits, adding one more variable to your debugging equation. Agilent Technologies' probes are mechanically designed to relieve strain and ensure a rugged and reliable connection.

Connectivity

A multitude of packages exist in the digital electronics industry. Check our large selection of probing solutions designed for specific chip packages or buses. As an alternative, we offer reliable termination adapters that work with standard on-target connectors.



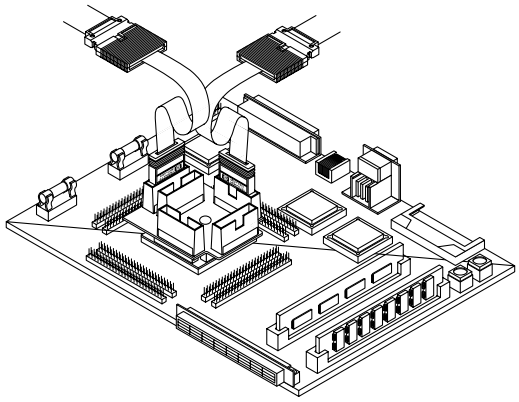


Figure 8. A rugged connection lets you capture accurate data; inverse assemblers help you make sense of it.

For more information refer to "Processor and Bus Support for Agilent Technologies Logic Analyzers."

Choose the Probing Technique That Best Fits Your Application

Probing your device under test is potentially one of the most difficult and certainly one of the most important tasks in debugging your digital design. That is why Agilent Technologies provides a wider variety of probing solutions than anyone else in the industry—each with a different set of advantages particular to a given situation. We like to think of it as helping you get your signals off to a great start.

Probing Alternative	Advantages	Limitations
General-Purpose Lead Sets and Surface Mount IC Clips (Figure 9 and 10)	Most flexible method. Works in conjunction with SMD clips and Wedge adapters listed below. Included with logic analyzer purchase.	Can be cumbersome when connecting a large number of channels.
Ultra-Fine Pitch Surface Mount Device Clips (Figure 11)	Smallest IC clips in the industry to date (down to 0.5 mm). Works with both logic analyzer and scope probing systems.	Same as above plus small incremental cost.
Wedge Probe Adapter for QFP Packages (Figure 12)	Compressible dual conductors between adjacent IC legs make 3-16 adjacent signal leads available to logic analyzer and scope probing systems.	Same as above plus small incremental cost.
Elastomeric Solutions for Generic QFP Packages (Figure 13)	Provides access to all signal leads for generic QFP packages (including custom ICs). Uses combination of one probe adapter and four flexible adapters, plus general-purpose lead sets.	Requires minimal keep out area. Moderate incremental cost.
Direct Connection to Device Under Test via Built-In Connectors (Figure 14 and 15)	Very reliable and convenient probing system when frequent probing connections are required (manufacturing or field test for example). Connectors can be located at optimal position in the device under test. Can work in conjunction with Agilent Technologies inverse assemblers.	Requires advance planning to integrate into design process. Moderate incremental cost.
Analysis Probes for Specific Processors and Buses (Figure 8)	Support for over 200 different processors and buses. Includes reliable logic analyzer probe pod connectors, logic analyzer configuration files and device-specific inverse assemblers.	Requires moderate clearance around processor or bus. Moderate to significant extra cost depending on specific processor or bus.

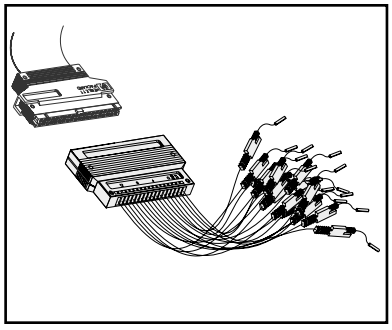


Figure 9. General-purpose probing solution

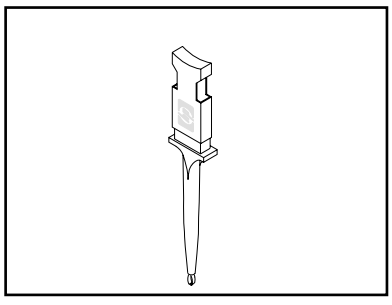


Figure 10. Surface mount IC clips

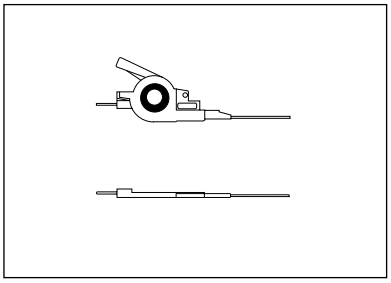


Figure 11. Ultra-fine pitch surface mount device clips

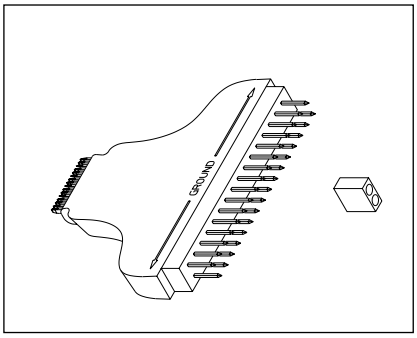


Figure 12. Agilent Wedge Probe Adapters for QFP package

Agilent Wedge Probe Adapter

IC leg spacing	Number of signals	Number of wedges in pack	Model number
0.5 mm	3	1	E2613A
0.5 mm	3	2	E2613B
0.5 mm	8	1	E2614A
0.5 mm	16	1	E2643A
0.65 mm	3	1	E2615A
0.65 mm	3	2	E2615B
0.65 mm	8	1	E2616A
0.65 mm	16	1	E2644A

Agilent Probing Solutions

Package type	Pin Pitch	Elastomeric Solutions
240-pin PQFP/CQFP	0.5 mm	E5363A probe adapter E5371A 1/4-flexible adapter
208-pin PQFP/CQFP	0.5 mm	E5374A probe adapter E5371A 1/4-flexible adapter
176-pin PQFP	0.5 mm	E5348A probe adapter E5349A 1/4-flexible adapter
160-pin QFP	0.5 mm	E5377A probe adapter E5349A 1/4-flexible adapter
160-pin PQFP/CQFP	0.65 mm	E5373A probe adapter E5349A 1/4-flexible adapter
144-pin PQFP/CQFP	0.65 mm	E5361A probe adapter E5340A 1/4-flexible adapter
144-pin TQFP	0.5 mm	E5336A probe adapter E5340A 1/4 flexible adapter

For more information refer to "Probing Solutions for Agilent Technologies Logic Analysis Systems."

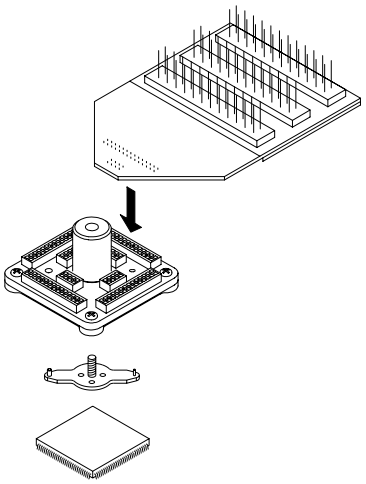


Figure 13. Elastomeric probing solution

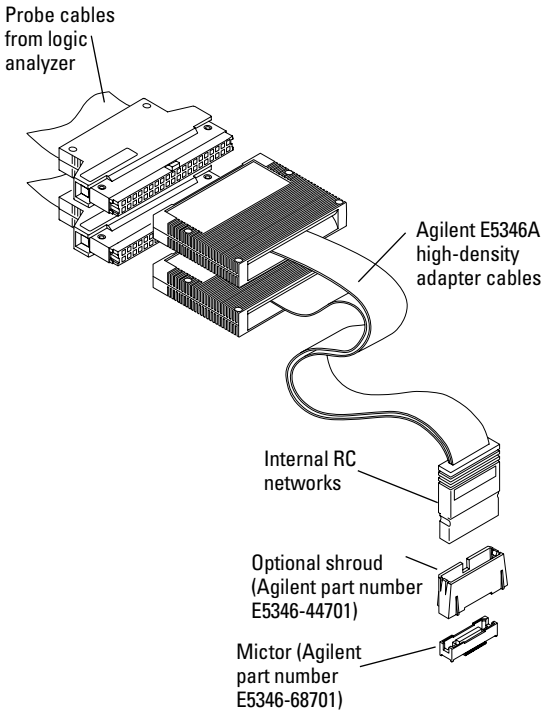


Figure 14. High-density direct connection solution

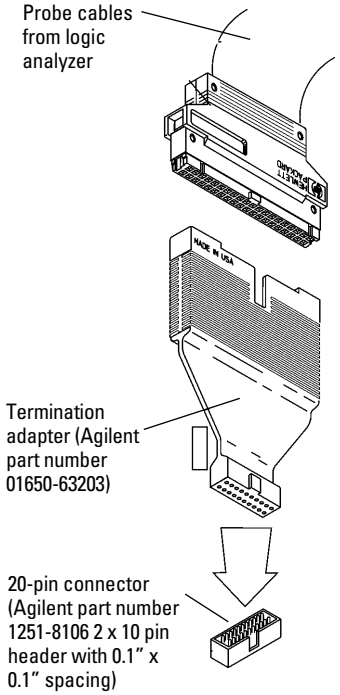


Figure 15. Normal-density direct connection solution

Examine Your Prototype's Behavior from All Angles

Causes and symptoms to problems often manifest themselves in different domains. Cross-module triggering and time correlation between state, timing, and analog measurements help you quickly gain insight to solve your tough hardware and software integration problems.

Track Problems in Multiprocessor Systems or Between a Processor and an Interface Bus

Configure any Agilent Technologies 1655X or 1671X Series module as two independent state analyzers that sample data using separate clocks. Then, view both time-correlated state listings together on the same screen.

Determine Whether the Problem is in Hardware or Software

Use our 2 GHz Timing Zoom to capture system behavior between states. Display both the state listing and Timing Zoom waveform and use the time-correlated markers to identify the cause of problem states.

Verify the Analog Behavior of a Signal at a Critical Time

Trigger the Agilent Technologies 16533A or 16534A digitizing oscilloscope from either the state or timing analyzer. Observe relationships among all three time-correlated measurements.

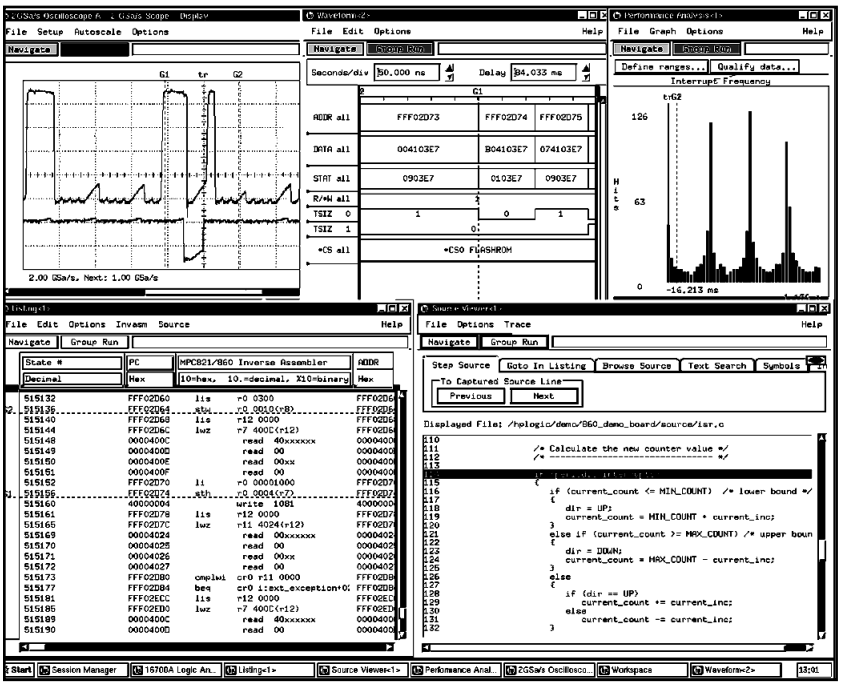


Figure 16. You can quickly isolate the root cause of system problems by examining target operation across a wide analysis domain, from analog signals to source code.

Debug Your Source Code

Now you can view high-level source code, time-correlated with the real-time logic analyzer trace, to provide a view into how the software actually executed in the system under test. The Agilent Technologies B4620B source correlation tool set links the logic analyzer trace with the source code that produced it.

Profile Your System's Performance

An optimized digital system requires a balance of hardware and software performance. The Agilent Technologies B4600B system performance analysis tool set allows you to profile your entire system to clearly identify bottlenecks in the hardware or software.

Display Options Supported in Agilent Technologies Logic Analysis Mainframes

Model	State/timing listing	State/timing waveform	State chart	Timing chart	State/timing distribution	State compare	Timing compare
16500C	√	√	√			√	
16700A, 16702A	√	√	√	√	√	√	√

A '√' indicates that the measurement is supported in the frame.

Analyze Target Operation with a Variety of Display Options

The Agilent Technologies logic analysis systems allow you to analyze target operation from different perspectives to help you identify problems quickly. In addition to the traditional state listing and timing waveform displays, you can view your data as a chart or a distribution over time.

Tools such as compare provide you with the ability to perform a bit-by-bit comparison between newly acquired data and a reference trace from a known working system. This quickly points you to any differences that are occurring between the two systems.

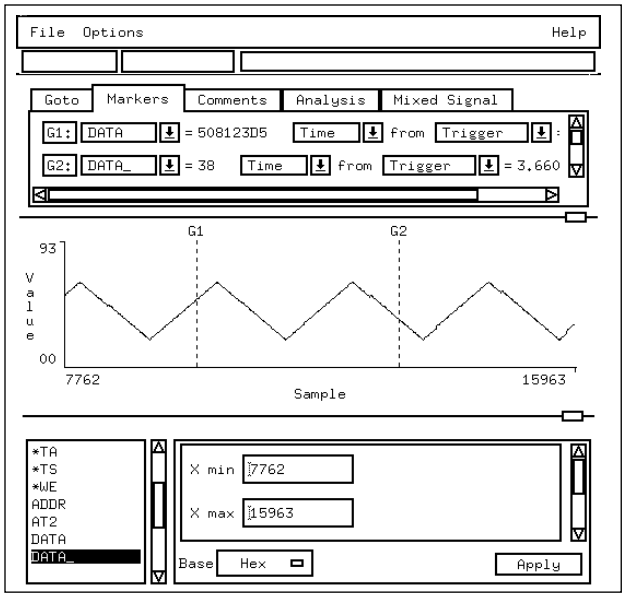


Figure 17. Verify A/D performance or track code flow graphically using the chart display.

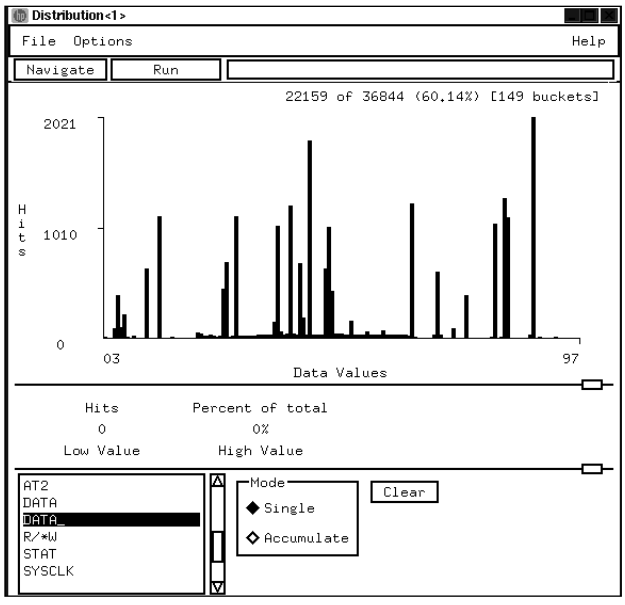


Figure 18. Analyze system performance to uncover bottlenecks in your hardware or software.

Agilent Technologies 16557D, 16710A, 16711A, 16712A Supplemental Specifications* and Characteristics

Probes (general-purpose lead set)

Input resistance	100 KΩ, ±2%
Parasitic tip capacitance	1.5 pF
Minimum voltage swing	500 mV, peak-to-peak
Threshold accuracy*	±(100 mV + 3% of threshold setting)
Maximum input voltage	±40 V peak

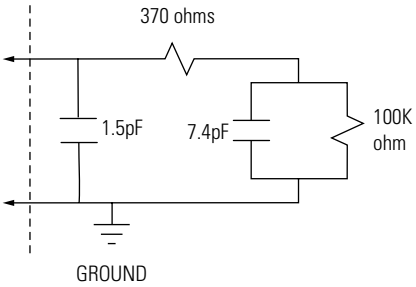


Figure 19. Equivalent probe load for the Agilent 16557D, 16710A, 16711A, and 16712A, general-purpose lead set.

State Analysis

Minimum state clock pulse width	3.5 ns
Time tag resolution [1]	8 ns
Maximum time count between states	34 seconds
Maximum state tag count between states [1]	4.29×10^9 states
Minimum master to master clock time*	16710A, 16711A, 16712A: 10 ns 16557D: 7.14 ns
Minimum master to slave clock time	0.0 ns
Minimum slave to master clock time	4.0 ns
Context store block sizes [2]	16, 32, 64 states

Timing Analysis

Sample period accuracy	0.01% of sample period
Channel-to-channel skew	2 ns, typical
Time interval accuracy	± (sample period + channel-to-channel skew + 0.01% of time interval reading)
Minimum detectable glitch	3.5 ns

Triggering

Maximum trigger sequence speed	125 MHz, maximum (Agilent 16710A/11A/12A) 140 MHz, maximum (Agilent 16557D)
Maximum occurrence counter	1,048,575
Range width	32 bits each
Timer value range	400 ns to 500 seconds
Timer resolution	16 ns or 0.1% whichever is greater
Timer accuracy	±32 ns or ±0.1% whichever is greater

Operating Environment

Temperature	Agilent 16600A series frame: Instrument, 0˚C to 40˚ C (+32˚F to 104˚F) Agilent 16700A series frame: Instrument 0˚C to 50˚C (+32˚F to 122˚F) Probe lead sets and cables, 0˚C to 65˚C (+32˚F to 149˚F)
Humidity	80% relative humidity at +40˚ C
Altitude	Operating 4600m (15,000ft) Nonoperating 15,300m (50,000ft)

[1] Time or state tags halve the acquisition memory when there are no unassigned pods.
[2] Only available with the Agilent 16710A , 16711A and 16712A modules.

Agilent Technologies 16517A/18A Supplemental Specifications* and Characteristics

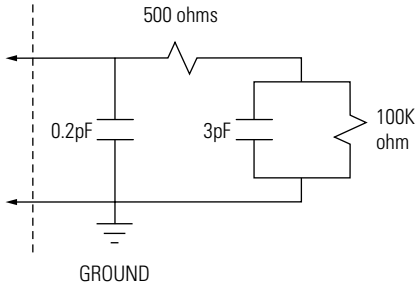


Figure 20. Equivalent probe load for the Agilent 16517A/18A.

Probes

Input dc resistance	100 KΩ, ±2%
Input impedance	dc thru 400 ns rise time, 100 KΩ typical 3.5 ns thru 350 ps, 500 Ω typical
Input capacitance	0.2 pF and then, through 500 Ω, 3 pF
Minimum voltage swing*	500 mV, peak-to-peak
Threshold accuracy*	±2% of input signal ±50 mV
Minimum input overdrive	250 mV or 30% of input (whichever is greater above the pod threshold)
Input dynamic range	±5 V above the threshold
Maximum input voltage	40 V peak-to-peak

Synchronous State Analysis

Minimum external clock period*	1 ns
Minimum state speed	20 MHz, requires a periodic clock
Minimum detectable pulse width	900 ps
Channel-to-channel skew	Per pod: 250 ps, typical Across pods: 1 ns, typical 250 ps, with manual adjustment
State clock duty cycle range	1 GHz thru 500 MHz: 45% - 55%, typical 500 MHz thru 250 MHz: 30% - 70%, typical 250 MHz thru 20 MHz: 20% - 80%, typical
Oversampling	2x, 4x, 8x, 16x, and 32x with a maximum rate of 2 GHz

Timing Analysis

Minimum detectable pulse width	4 GHz: 800 ps, typical 2 GHz or less: 1.1 ns, typical
Sample period accuracy	0.005% of sample period
Channel-to-channel skew	250 ps across all channels, typical
Time interval accuracy	± (sample period + channel-to-channel skew + 0.005% of time interval reading)

Trigger Characteristics

Maximum sequencer speed	500 MHz
Maximum occurrence count	16,777,216
Minimum pattern recognizer pulse width	2.25 ns
Edge counting frequency	444 MHz
Edge detection	Up to 1 GHz
Greater than duration (timing only)	0 ns to 510 ns range, accuracy is ±2.25 ns
Less than duration (timing only)	4 ns to 510 ns range, accuracy is ±2.25 ns
Timer/counter range	Timing mode: 0 s to 33 ms State mode: 500 MHz to 1 GHz, (user clock period) x (2^{23}) Below 500 MHz, (user clock period) x (2^{24})
Timer resolution	Timing mode: 2 ns State mode: Above 500 MHz, 2 x (user clock period) Below 500 MHz, user clock period
Timer accuracy	0.005% of timer value

Agilent Technologies 16715A, 16716A, 16717A, 16718A, 16719A Supplemental Specifications* and Characteristics

Probes (general-purpose lead set)

Input resistance	100 KΩ, ± 2%
Parasitic tip capacitance	1.5 pF
Minimum voltage swing	500 mV, peak-to-peak
Minimum input overdrive	250 mV
Threshold range	-6V to +6V in 10 mV increments
Threshold accuracy*	± (65 mV + 1.5% of settings)
Input dynamic range	± 10V about threshold
Maximum input voltage	± 40V peak
+5V Accessory current	1/3 amp maximum per pod
Channel assignment	Each group of 34 channels can be assigned to Analyzer 1, Analyzer 2 or remain unassigned

2 GHz Timing Zoom (Agilent 16716A, 16717A, 16718A, 16719A only)

Timing analysis sample rate	2 GHz/1 GHz/500 MHz/250 MHz
Sample period accuracy	± 50 ps
Channel-to-channel skew	< 1.0 ns
Time interval accuracy	± (sample period + channel-to-channel skew + 0.01% of time interval reading)
Memory depth	16 K
Trigger position	Start, center, end, or user defined

Operating Environment

Temperature	Agilent 16700A Series frame: 0˚C to 50˚C (+32˚F to 122˚F) Probe lead sets and cables: 0˚C to 65˚C (+32˚F to 149˚F)
Humidity	80% relative humidity at + 40˚C
Altitude	Operating 4600 m (15,000 ft) Non-operating 15,300 m (50,000 ft)

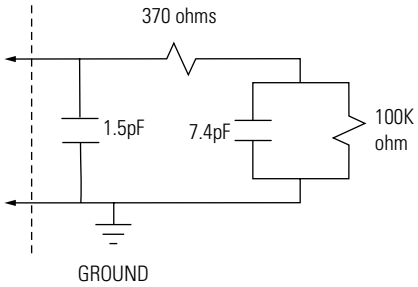


Figure 21. Equivalent probe load for the Agilent 16715A, 16716A, 16717A, 16718A, 16719A general-purpose lead set.

Agilent Technologies 16715A, 16716A, 16717A, 16718A, 16719A Supplemental Specifications* and Characteristics (cont'd)

167 MHz State Mode

Maximum state speed*	167 MHz
Channel count	68 per module
Maximum channels on a single time base and trigger	340
Number of independent analyzers	2, can be setup in state or timing modes
Minimum master to master clock time* [1]	5.988 ns
Minimum master to slave clock time	2 ns
Minimum slave to master clock time	2 ns
Minimum slave to slave clock time	5.988 ns
Setup/hold time* [1] (single-clock, single-edge)	2.5 ns window adjustable from 4.5/-2.0 ns to -2.0/4.5 ns in 100 ps increments per channel
Setup/hold time* [1] (multi-clock, multi-edge)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
Setup/hold time (with manual adjustment)	1.0 ns window
Minimum state clock pulse width	1.2 ns
Time tag resolution [2]	4 ns
Maximum time count between states	17 seconds
Maximum state tag count between states [2]	2^{32}
Number of state clocks/qualifiers	4
Maximum memory depth	16716A: 512K 16715A, 16717A: 2M 16718A: 8M 16719A: 32M
Maximum trigger sequence speed	167 MHz
Maximum trigger sequence levels	16
Trigger sequence level branching	4 way arbitrary "IF/THEN/ELSE" branching
Trigger position	Start, center, end, or user defined

Agilent Technologies 16715A, 16716A, 16717A, 16718A, 16719A Supplemental Specifications* and Characteristics (cont'd)

167 MHz State Mode (cont'd)

Trigger resources	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 8 Flags
Trigger resource conditions	Arbitrary boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and goto Store/don't store sample Turn on/off default storing Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear
Store qualification	Default and per sequence level
Maximum global counter	16,777,215
Maximum occurrence counter	16,777,215
Maximum pattern/range width	32 bits
Timers value range	100 ns to 5497 seconds
Timer resolution	5 ns
Timer accuracy	10 ns + .01%
Timer reset latency	70 ns
Data in to trigger out (BNC port)	150 ns, typical
Flag set/reset to evaluation	110 ns, typical

Agilent Technologies 16715A, 16716A, 16717A, 16718A, 16719A Supplemental Specifications* and Characteristics (cont'd)

333 MHz State Mode (Agilent 16717A, 16718A, 16719A only)

Maximum state speed*	333 MHz
Channel count	(Number of modules x 68) - 34
Maximum channels on a single time base and trigger	306
Number of independent analyzers	1, when 333 MHz state mode is selected the second analyzer is turned off
Minimum master to master clock time* [1]	3.003 ns
Setup/hold time* [1] (single-clock, single-edge)	2.5 ns window adjustable from 4.5/-2.0 ns to-2.0/4.5 ns in 100 ps increments per channel
Setup/hold time* [1] (single-clock, multi-edge)	3.0 ns window adjustable from 5.0/-2.0 ns to -1.5/4.5 ns in 100 ps increments per channel
Setup/hold time (with manual adjustment)	1.0 ns window
Minimum state clock pulse width	1.2 ns
Time tag resolution [2]	4 ns
Maximum time count between states	17 seconds
Number of state clocks	1
Maximum memory depth	16717A: 2M 16718A: 8M 16719A: 32M
Maximum trigger sequence speed	333 MHz
Maximum trigger sequence levels	15
Trigger sequence level branching	Dedicated next state branch or reset
Trigger position	Start, center, end, or user defined
Trigger resources	8 Patterns evaluated as =, ≠, >, <, ≥, ≤ 4 Ranges evaluated as in range, not in range 2 Occurrence counters 8 Flags
Trigger resource conditions	Arbitrary boolean combinations
Trigger actions	Goto Trigger and fill memory
Store qualification	Default
Maximum occurrence counter	16,777,215
Maximum pattern/range width	32 bits
Data in to trigger out (BNC port)	150 ns, typical
Flag set/reset to evaluation	110 ns, typical

Agilent Technologies 16715A, 16716A, 16717A, 16718A, 16719A Supplemental Specifications* and Characteristics (cont'd)

Timing Mode

Timing analysis sample rate (full/half channel)	333/667 MHz
Channel count	68 per module
Maximum channels on a single time base and trigger	340
Number of independent analyzers	2, can be setup in state or timing modes
Sample period (full channel)	3 ns to 1 ms
Sample period (half channel)	1.5 ns
Sample period accuracy	±(100 ps + .01% of sample period)
Channel-to-channel skew	< 1.5 ns
Time interval accuracy	± (sample period + channel-to-channel skew + .01% of time interval reading)
Minimum detectable glitch	1.5 ns
Memory depth (full/half channel)	16716A: 512K/1M 16715A, 16717A: 2/4M 16718A: 8/16M 16719A: 32/64M
Maximum trigger sequence speed	167 MHz
Maximum trigger sequence levels	16
Trigger sequence level branching	4 way arbitrary "IF/THEN/ELSE" branching
Trigger position	Start, center, end, or user defined
Trigger resources	16 Patterns evaluated as =, ≠, >, <, ≥, ≤ 15 Ranges evaluated as in range, not in range 2 Edge/glitch (2 Timers per module) -1 2 Global counters 1 Occurrence counter per sequence level 8 Flags
Trigger resource conditions	Arbitrary boolean combinations
Trigger actions	Goto Trigger and fill memory Trigger and goto Timer start/stop/pause/resume Global counter increment/reset Occurrence counter reset Flag set/clear
Maximum global counter	16,777,215
Maximum occurrence counter	16,777,215
Maximum pattern/range width	32 bits
Timer value range	100 ns to 5497 seconds
Timer resolution	5 ns
Timer accuracy	±10 ns + .01%
Greater than duration	6 ns to 100 ms in 6 ns increments
Less than duration	12 ns to 100 ms in 6 ns increments
Timer reset latency	70 ns
Data in to trigger out (BNC port)	150 ns, typical
Flag set/reset to evaluation	110 ns, typical

[1] Specified for an input signal VH=-0.9V, VL=-1.7V, Slew rate=1V/ns, and threshold=-1.3V.
[2] Time or state tags halve the acquisition memory when there are no unassigned pods.

Related Agilent Technologies Literature

Refer to the documents below for more information on Agilent Technologies logic analysis systems and accessories.

Publication Titles	Publication Type	Publication Number
HP 16600A and 16700A Series Logic Analysis Mainframes	Product Overview	5966-3107E
Oscilloscope Modules for HP Logic Analysis Systems	Product Overview	5966-3150E
HP 16522A 200 mVector/sec Pattern Generator Module for HP Logic Analysis	Product Overview	5964-2250E
Post Processing Tool Sets for the HP 16600A and 16700A Series Logic Analysis Systems	Product Overview	5966-3147E
Emulation and Analysis Solutions for the Motorola MPC 8XX Microprocessors	Product Overview	5966-2866E
Passively Probing a Motorola MPC 860/821 BGA Target System with HP E5346A High-Density Termination Adapters	Product Note	5966-4165E
Emulation and Analysis Solutions for the Motorola PPC 6XX Microprocessors	Product Overview	5966-2868E
Emulation and Analysis Solutions for the Motorola/IBM Power PC 740/750 Microprocessors	Product Overview	5966-2867E
Emulation and Analysis Solutions for Intel Pentium II Processors with MMX Technology	Product Overview	5966-3880E
HP E2487C Analysis Probe & HP E2492B/C/D Probe Adapter for Intel Celeron, Pentium II/III and Pentium II/III Xeon Processors	Product Overview	5968-2421E
Emulation and Analysis Solutions for Intel Pentium Processors and Pentium Processors with MMX Technology	Product Overview	5966-3106E
Emulation and Analysis Solutions for ARM7 and ARM9 Microprocessors	Product Overview	5966-3442E
Probing Solutions for HP Logic Analysis Systems	Product Overview	5968-4632E
Processor and Bus Support for Agilent Technologies Logic Analyzers	Configuration Guide	5966-4365E

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State and Timing Module	Logic Analysis System Frame	
	16500C, 16501A	16700A, 16701A, 16702A
16517A , 16518A	√	√
16557D	√	√
16710A		√
16711A		√
16712A		√
16715A		√
16716A		√
16717A		√
16718A		√
16719A		√

A '√' = indicates the module is supported in the frame.

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