Agilent Technologies InfiniiVision MSO N5406A FPGA Dynamic Probe for Xilinx

Data Sheet

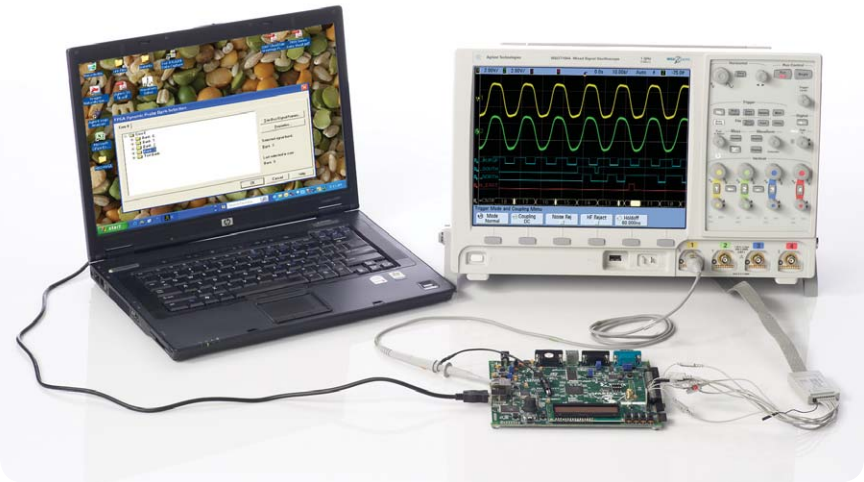


Figure 1. FPGA dynamic probe for Xilinx used in conjunction with an Agilent InfiniiVision 6000 or 7000 Series MSO provides an effective solution for simple through complex debugging of systems incorporating Xilinx FPGAs.

The challenge

You rely on the insight a MSO (mixed-signal oscilloscope) provides to understand the behavior of your FPGA in the context of the surrounding system. Design engineers typically take advantage of the programmability of the FPGA to route internal nodes to a small number of physical pins for debugging. While this approach is very useful, it has significant limitations.

- Since pins on the FPGA are typically an expensive resource, there are a relatively small number available for debug. This limits internal visibility (i.e. one pin is required for each internal signal to be probed).

- When you need to access different internal signals, you must change your design to route these signals to the available pins. This can be time consuming and can affect the timing of your FPGA design.

- Finally, the process required to map the signal names from your FPGA design to the MSO digital channel labels is manual and tedious.

  When new signals are routed out, you need to manually update these signal names on the MSO, which takes additional time and is a potential source of confusing errors.

Debug your FPGAs faster and more effectively with a MSO

A better way – Collaborative development between Agilent and Xilinx have produced a faster and more effective way to use your MSO to debug FPGAs and the surrounding system. The Agilent FPGA dynamic probe, used in conjunction with an Agilent MSO, provides the most effective solution for simple through complex debugging.

View internal activity – With the digital channels on your MSO, you are normally limited to measuring signals at the periphery of the FPGA. With the FPGA dynamic probe, you can now access signals internal to the FPGA. You can measure up to 64 internal signals for each external pin dedicated to debug, unlocking visibility into your design that you never had before.

Make multiple measurements in seconds – Moving probe points internal to an FPGA used to be time consuming. Now, in less than a second, you can easily measure different sets of internal signals without design changes. FPGA timing stays constant when you select new sets of internal signals for probing.

Leverage the work you did in your design environment – The FPGA dynamic probe maps internal signal names from your FPGA design tool to your Agilent MSO. Eliminate unintentional mistakes and save hours of time with this automatic setup of signal and bus names on your MSO.

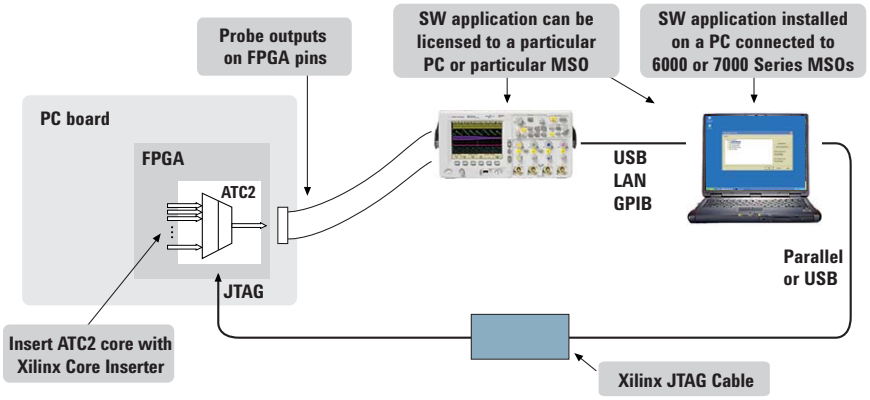


Figure 2. Create a timesaving FPGA measurement system. Insert an ATC2 (Agilent Trace Core) core into your FPGA design. With the application running on your PC you control which group of internal signals to measure via JTAG.

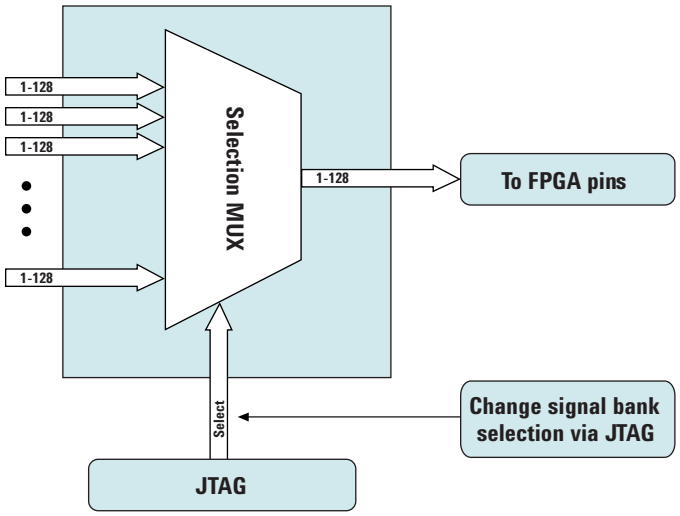
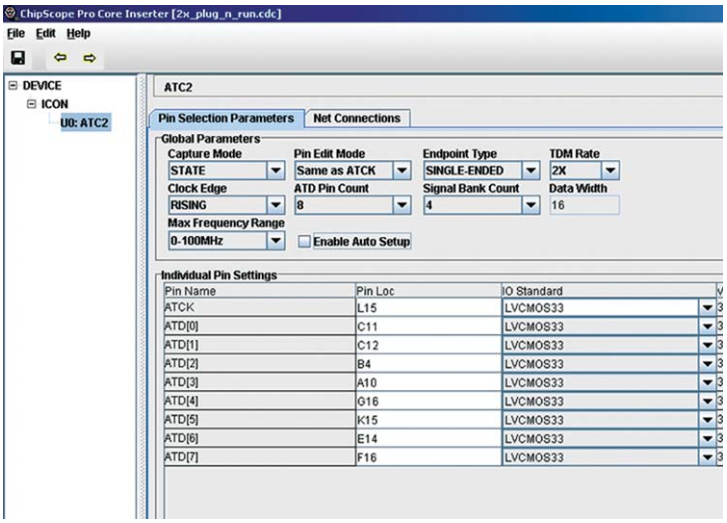


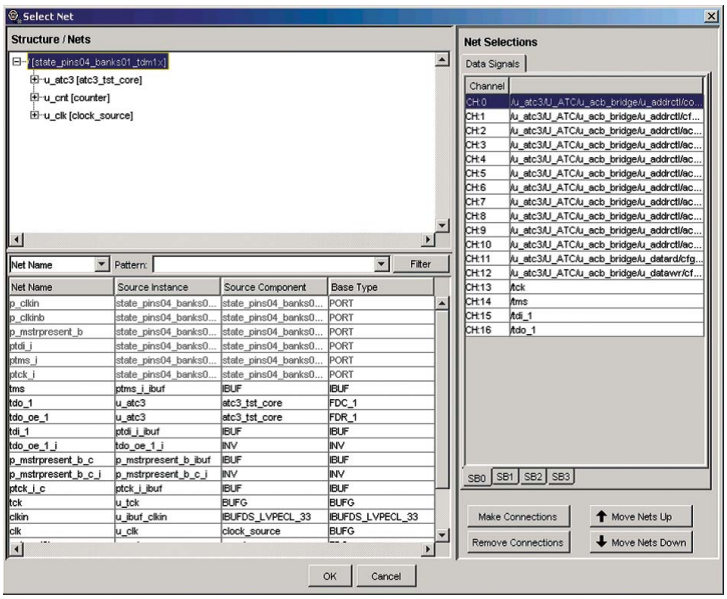
Figure 3. Access up to 64 internal signals for each debug pin. Signal banks all have identical width (1 to 128 signals wide) determined by the number of device pins you devote for debug. Each pin provides sequential access to one signal from every input bank.

A quick tour of the application

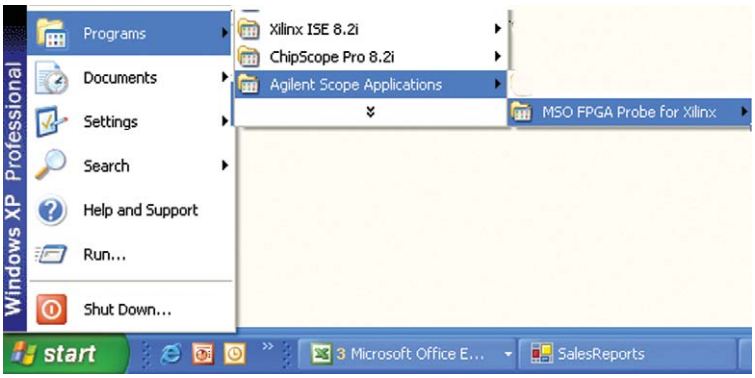
Design step 1: Create the ATC2 core
Use Xilinx Core Inserter or EDK to select your ATC2 parameters and to create a debug core that best matches your development needs. Parameters include number of pins, number of signal banks, the type of measurement (state or timing), and other ATC2 attributes.



Design step 2: Select groups of signals to probe
Specify banks of internal signals that are potential candidates for MSO measurements (using Xilinx Core Inserter or EDK).

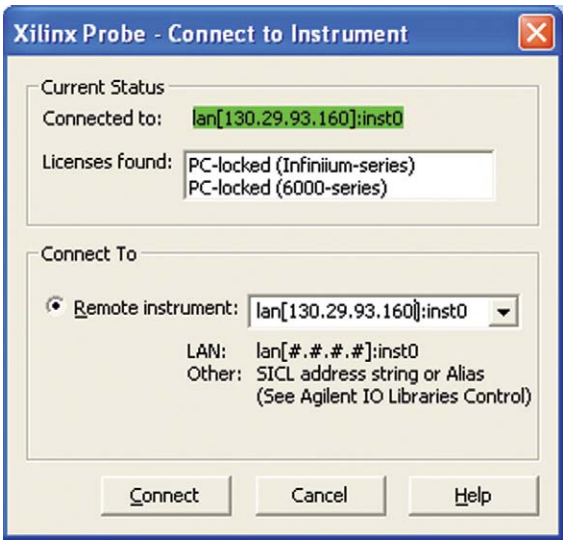


Activate FPGA dynamic probe for Xilinx
The FPGA dynamic probe application allows you to control the ATC2 core and set up the MSO for the desired measurements. This application runs on a PC.

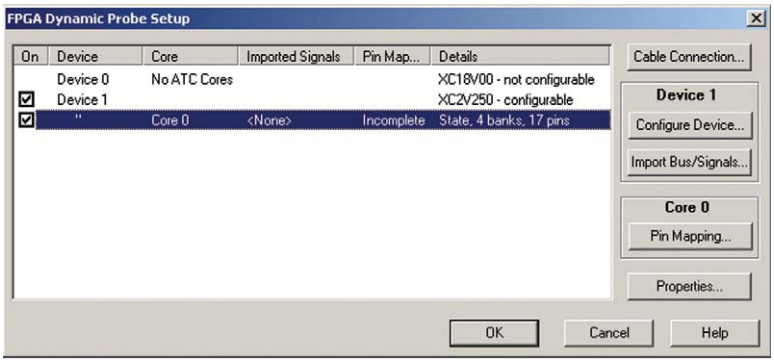


A quick tour of the application (continued)

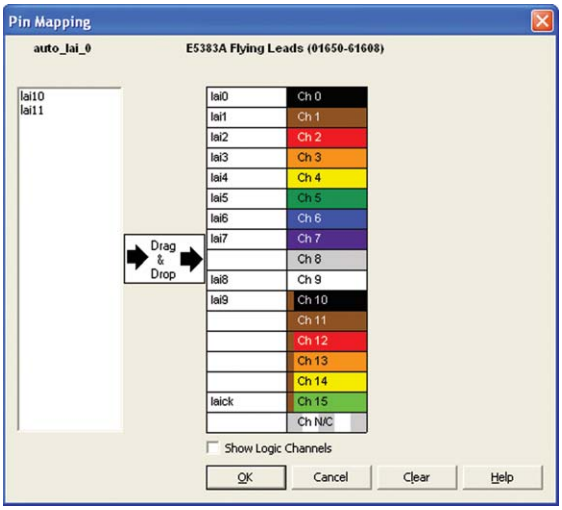
Connect your MSO to your PC
From FPGA dynamic probe application software, specify the communication link between your PC and MSO.



Measurement setup step 1: Establish a connection between the PC and the ATC2 core
The FPGA dynamic probe application establishes a connection between the PC and a Xilinx cable. It also determines what devices are on the JTAG scan chain and lets you pick which one you wish to communicate with. Core and device names are user definable.

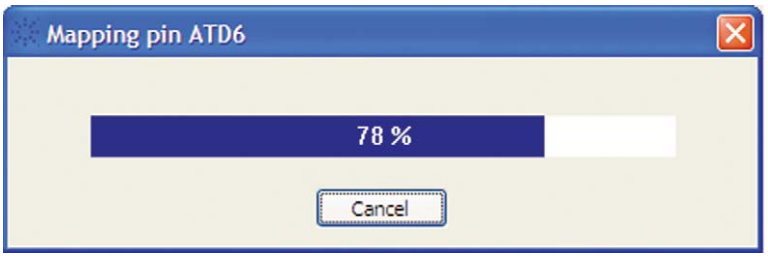


Measurement setup step 2: Map FPGA pins
Quickly specify how the FPGA pins (the signal outputs of ATC2) are connected to your MSO. Select your probe type and rapidly provide the information needed for the MSO to automatically track names of signals routed through the ATC2 core.



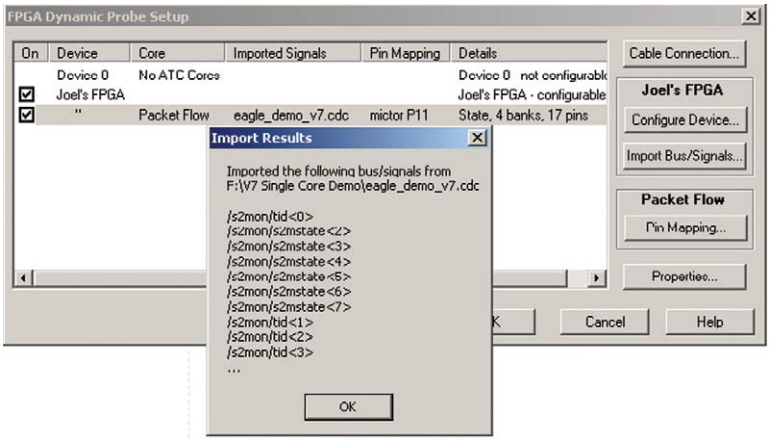
A quick tour of the application (continued)

For ATC2 cores with auto setup enabled, each pin of the ATC2 core, one at a time, produces a unique stimulus pattern. The instrument looks for this unique pattern on any of its acquisition channels. When the instrument finds the pattern, it associates that instrument channel with the ATC2 output pin producing it. It then repeats the process for each of the remaining output pins eliminating the need to manually enter probe layout information.



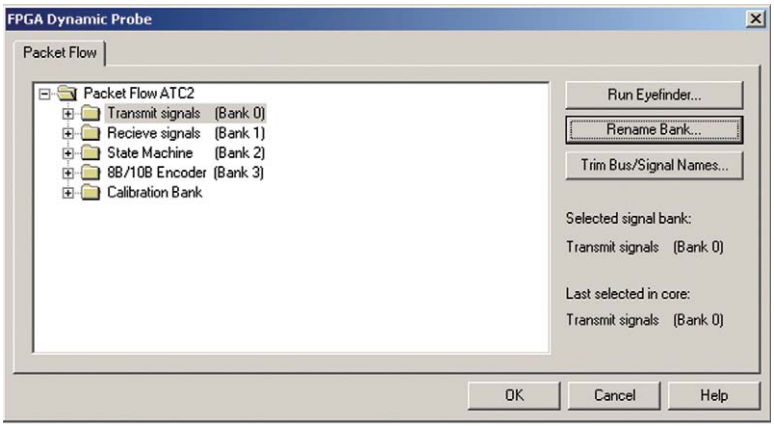
Measurement setup step 3: Import signal names

Tired of manually entering bus and signal names on your MSO? The FPGA dynamic probe application reads a .cdc file produced by Xilinx Core Inserter. The names of signals you measure will now automatically show on your MSO digital channel labels.



Setup complete: Make measurements

Quickly change which signal bank is routed to the MSO. A single mouse click tells the ATC2 core to switch to the newly specified signal bank without any impact to the timing of your design. To make measurements throughout your FPGA, change signal banks as often as needed. User-definable signal bank names make it straight forward to select a part of your design to measure.



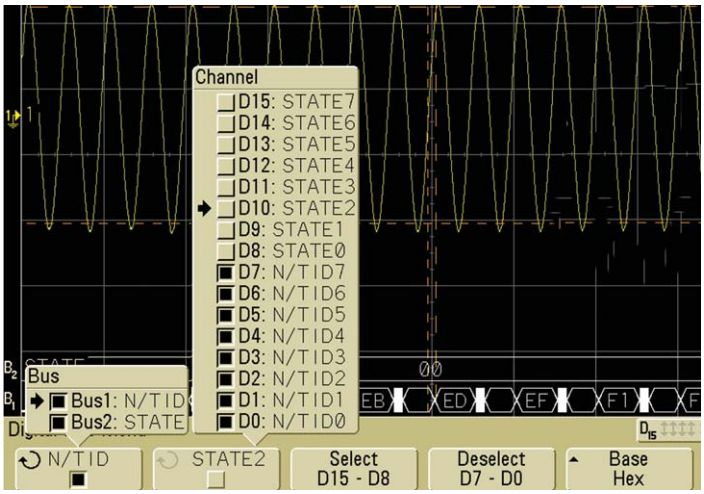
A quick tour of the application (continued)

Triggering on valid states

MSOs incorporate logic state triggering for triggering on specific states. Set up a valid state trigger by specifying the clock edge and the desired bus/signal pattern. Because the ATC2 core outputs both the clock signal and bus values, triggering on the combination ensures your state trigger is valid—even though the digital channels are sampling asynchronously. Track valid states by measuring the bus value on each falling clock edge for image shown.

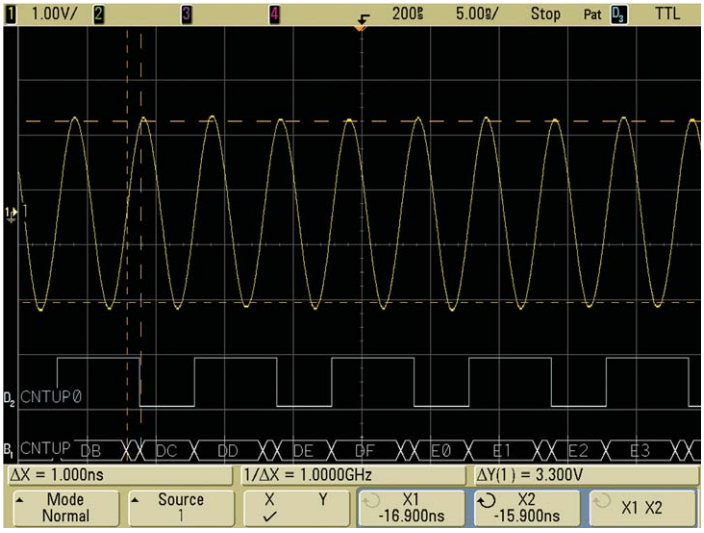
Automatic bus groupings

InfiniiVision MSOs include up to 2 bus groupings. Contiguous signal names are automatically grouped and displayed as buses. Bus values can be displayed as HEX or binary values. Additional signals are shown using independent waveforms.



Correlate internal FPGA activity with external measurements

View internal FPGA activity and time-correlate internal FPGA measurements with external analog and digital events in the surrounding system. FPGA Dynamic Probe unlocks the power of the MSO for system-level debug with FPGAs.



Agilent N5406A specifications and characteristics

Supported logic analyzers

Standalone oscilloscopes	InfiniiVision 6000 and 7000 Series MSOs
MSO Digital Channels	16
Bus groupings	Up to 2, each with 6 character labels
Triggering capabilities	Determined by MSO, all have state triggering
Supported Xilinx FPGA families	Virtex-6, Virtex-5, Virtex-4, Spartan-3, Spartan-6
Supported Xilinx cables (required)	Parallel 3 and 4, Platform Cable USB
Supported probing mechanisms	Soft touch (34-channel and 17-channel), Mictor, Samtec, Flying lead, 6000 and 7000 Series MSOs come standard with a 40 pin probe cable and flying leads. Cables and probing for Mictor, soft touch, or Samtec probing must be purchased separately.

Agilent trace core characteristics

Number of output signals	User definable: Clock line plus 4 to 128 signals in 1 signal increments
Signal banks	User definable: 1, 2, 4, 8, 16, 32, or 64
Modes	State (synchronous) or timing (asynchronous) mode
FPGA Resource consumption	Approximately 1 slice required per input signal to ATC2 Core Consumes no BUFGs, DCM or Block RAM resources. See resource calculator at **www.agilent.com/find/fpga**

Compatible design tools

ChipScope Pro version	Agilent MSO FPGA dynamic probe SW version	Primary new features
6.2i, 6.3i	1.0 or higher	Mouse-click bank select, graphical pin mapping, cdc signal name import
7.1i	2.03 or higher	Plug & run (auto pin mapping), ATC2 "always on" option, ATC2 width + 64 banks, Platform Cable USB support, PRBS stimulus on test bank
11.4	2.4	Added support for Virtex-6, Virtex-5 and Spartan-6 devices. Removal of Virtex II support.
EDK (Embedded Development Kit) 8.1i SP2	2.03 or higher	Support for ATC2 core using EDK flow
Synthesis		Core Inserter produces ATC2 cores post-synthesis (pre-place and route) making the cores synthesis independent. ATC2 cores produced by Core Generator are compatible with: • Exemplar Leonardo Spectrum • Synopsys Design Compiler • Synopsys Design Compiler II • Synopsys FPGA Express • Synplicity Synplify • Xilinx XST

Additional information available via the Internet: **www.agilent.com/find/FPGA** and **www.agilent.com/find/7000-xilinx**.

Ordering information

Ordering options for the Agilent N5405A FPGA dynamic probe for Xilinx

Option 001	• Entitlement certificate for perpetual node-locked license locked to oscilloscope (most common).
Option 002	• Entitlement certificate for PC locked license. PC and MSO must both connect to LAN. USB, or GPIB (fewer users order this license type)

Related literature

Publication title	Publication type	Publication number
Frequently Asked Questions MSO FPGA Dynamic Probe for Xilinx	Data Sheet	5989-5976EN
Agilent Technologies 6000 Series Oscilloscopes	Data Sheet	5989-2000EN
Agilent Technologies InfiniiVision 7000 Series Oscilloscopes	Data Sheet	5989-7736EN

Product Web site

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