The HP 1660-Series Benchtop Logic Analyzers

Technical Data

Finding the cause of difficult problems fast.

There is little room for error in the schedules for design projects today. You need test equipment that can locate the cause of a problem quickly and with certainty.

The HP 1660-series logic analyzers help you rapidly troubleshoot elusive hardware failures, verify proper bus operation, and debug software during real-time execution.

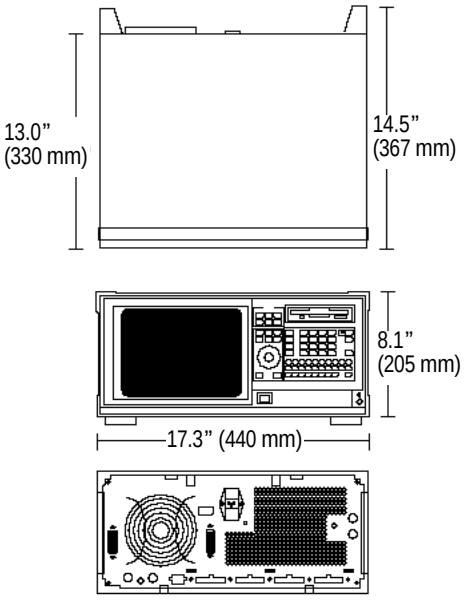
Choose a model with 34, 68, 102 or 136 logic analyzer channels. They all have enough timing and state analysis speed to handle even high-performance applications. Then consider adding a built-in, 2-channel oscilloscope to show signal parametrics – especially when the logic analyzer locates a failure.

We think you will agree that these logic analyzers have the right combination of performance, flexibility, and ease of use to help you solve difficult problems fast.

- Graphical menus are displayed on a gray-scale CRT
- Front-panel keypad, mouse and optional keyboard human interfaces
- 3.5 inch high-density flexible disk drive supports LIF and DOS formats
- New, advanced inverse assemblers
- Store data as ASCII files and screen images in TIFF, PCX and PostScript™ formats
- New, graphical trigger macros make trigger setup easier
- Fully programmable

PostScript™ is a trademark of Adobe Systems Incorporated.

Product Specifications and Characteristics



Weight 26 lbs. (11.8 kg)

Figure 1

Logic Analyzer Key Specifications and Characteristics

Model Number	HP 1660A,AS	HP 1661A,AS	HP 1662A,AS	HP 1663A,AS	HP 1664A
State and Timing Channels	136	102	68	34	34
Timing Analysis	Conventional: 250 MHz all channels, 500 MHz half channels Transitional: 125 MHz all channels, 250 MHz half channels Glitch: 125 MHz half channels				
State Analysis Speed	100 MHz, all channels				50 MHz
State Clocks/ Qualifiers	6	6	4	2	2
Memory Depth per Channel	4K per channel, 8K in half-channel modes				

Oscilloscope Key Specifications and Characteristics

Model Number	HP 1660AS, HP 1661AS, HP 1662AS & HP 1663AS
Channels	2
Maximum Sample Rate	1 GSa/s per channel
Bandwidth	dc to 250 MHz (dc coupled)
Rise Time	1.4 ns
Vertical Resolution	8 bits
Memory Depth per Channel	8k samples

Model Number	Logic Analyzer Channels	Built-in, 2-Channel Oscilloscope
HP 1660A	136	No
HP 1660AS	136	Yes
HP 1661A	102	No
HP 1661AS	102	Yes
HP 1662A	68	No
HP 1662AS	68	Yes
HP 1663A	34	No
HP 1663AS	34	Yes
HP 1664A	34	No

Human Interface

Front Panel — A knob and keypads make up the front-panel human interface. Keys include control, menu, display navigation, and alpha-numeric entry functions.

Mouse — An HIL, 3-button mouse (HP p/n A2838A) is shipped as standard equipment. It provides full instrument control. Knob functionality is replicated by holding down the center button and moving the mouse left or right.

Keyboard — The logic analyzer can also be operated using an HIL keyboard. Order the HP Logic Analyzer Keyboard Kit, model number E2427A.

Input/Output, Control, and Printing

I/O Ports — The HP 1664A ships with a parallel (Centronics) printer port as standard equipment; RS-232 and HP-IB ports are optional. All other models ship with RS-232 and HP-IB as standard equipment but do not have a parallel port.

Programmability — Each instrument is fully programmable from a computer via HP-IB and RS-232 connections. This feature is standard on all models except the HP 1664A. Order option 020 for HP 1664A programmability.

HP Printer Support — Printers which use the HP Printer Control Language (PCL) and have an HP-IB, RS-232 or parallel* interface are supported: HP DeskJet, LaserJet, QuietJet, PaintJet, and ThinkJet models.
* HP 1664A only

Alternate Printer Supported — The Epson FX80, LX80 and MX80 printers with an RS-232 interface are supported in the Epson 8-bit graphics mode.

Hard Copy Output — Screen images can be printed in black and white from all menus using the *Print* field. State or timing listings can be also be printed in full or part (starting from center screen) using the *Print All* selection.

Mass Storage Files and Software

Updating the Operating System — For models other than the HP 1664A, the operating system resides in Flash ROM and can be updated from the flexible disk drive. The HP 1664A boots from disk and requires only a disk change to update the operating system.

Mass Storage — A high density (1.44-Mbyte), 3.5" flexible disk drive supports LIF and DOS formats.

Screen Image Files — An image file of any display screen can be stored to disk via the display's *Print* field. Black & white TIFF, PCX, PostScript, and gray-scale TIFF file formats are available.

ASCII Data Files — State or timing listings can be stored as ASCII files on a flexible disk via the display's *Print* field. These files are equivalent in character width and line length to hard-copy listings printed via the *Print All* selection.

Configuration and Data Files — Logic analyzer and oscilloscope files that include configuration and data information (if present) are encoded in a binary format. They can be stored to or loaded from a flexible disk.

Recording of Acquisition and Storage Times — Binary format configuration/data files are stored with the time of acquisition and the time of storage for all models except the HP 1664A, which does not have a real-time clock.

Acquisition Arming

Initiation — Arming is started by *Run, Group Run,* or the Port In BNC.

Cross Arming — Analyzer machines and the oscilloscope can cross-arm each other.

Output — An output signal is provided at the Port Out BNC.

Port In/Out

PORT IN Signal and Connection — Port In is a standard BNC connection. The input operates at TTL logic signal levels. Rising edges are valid input signals.

PORT OUT Signal and Connection — Port Out is a standard BNC connection with TTL logic signal levels. A rising edge is asserted as a valid output.

Skew Adjustment and Arming Times

Skew Adjustment — Correction factors for nominal skew between displayed timing and oscilloscope signals are built into the operating system. Additional correction for unit-by-unit variation can be made using the *Skew* field. An entered skew value affects the next (not the present) acquisition display.

HP 1660-series Logic Analyzer Specifications and Characteristics

PORT IN Arms Logic Analyzer [1]	15 ns typical delay from signal input to a *don't care* logic analyzer trigger.
PORT IN Arms Oscilloscope	40 ns typical delay from signal input to an *immediate* oscilloscope trigger; not available when oscilloscope is in time-qualified pattern triggering mode.
Logic Analyzer Arms PORT OUT [1]	120 ns typical delay from logic analyzer trigger to signal output.
Oscilloscope Arms PORT OUT	60 ns typical delay from oscilloscope trigger to signal output.

Operating Environment

Power	115 Vac or 230 Vac, –22% to +10%, single phase, 48-66 Hz, 320 VA max
Temperature	Instrument, 0° to 50° C (+32° to 122° F). Disk media, 10° to 40° C (+50° to 104°F). Probes and cables, 0° to 65° C (+32° to 149° F)
Humidity	Instrument, up to 95%, relative humidity at +40° C (+140° F). Disk media, 8% to 80% relative humidity.
Altitude	To 460 m (15,000 ft)
Vibration: Operating	Random vibrations 5-500Hz, 10 minute per axis, ~ 0.3 g (rms).
Vibration: Non Operating	Random vibrations 5-500Hz, 10 minutes per axis,~ 2.41 g (rms); and swept sine resonant search, 5-500 Hz, 0.75 g (0-peak), 5 minute resonant dwell @ 4 resonances per axis.

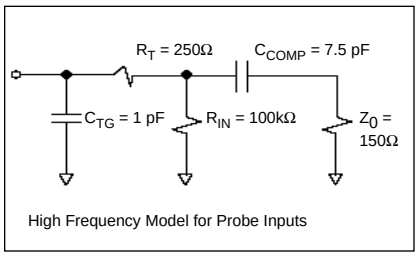
Physical Factors

Weight	26 lbs.. (11.8 kg)
Dimensions	See figure 1 on pg. 1
Safety	IEC 348/ HD 401, UL 1244, and CSA Standard C22.2 No. 231 (series M-89)

EMC
CISPR 11:1990/EN 55011 (1991):
Group 1 Class A
IEC 801-2:1991/EN 50082-1 (1992):
4kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m
IEC 801-4:1988/EN 50082-1 (1992): 1kV

Logic Analyzer Probes

Input Resistance	100 kΩ ±2%
Input Capacitance	approx. 8 pF (see figure)



High Frequency Model for Probe Inputs

Minimum Input Voltage Swing	500 mV peak-to-peak
Minimum Input Overdrive	250 mV or 30% of input amplitude, whichever is greater
Threshold Range	–6.0 V to +6.0 V in 50-mV increments
Threshold Setting	Threshold levels may be defined for pods (17-channel groups) on an individual basis
Threshold Accuracy*	± (100 mV +3% of threshold setting)
Input Dynamic Range	± 10 V about the threshold
Maximum Input Voltage	± 40 V peak
+5 V Accessory Current	1/3 amp maximum per pod
Channel Assignment	Each group of 34 channels (a pod pair) can be assigned to Analyzer 1, Analyzer 2 or remain unassigned.

State Analysis

Maximum State Speed*	100 MHz all models except HP 1664A, which is 50 MHz	
Channel Count [1]	HP 1660A, AS	136/68
	HP 1661A, AS	102/51
	HP 1662A, AS	68/34
	HP 1663A, AS	34/17
	HP 1664A	34/17
Memory Depth per Channel [1]	4096/8192 samples	
State Clocks	HP 1660A, AS	6 clocks
	HP 1661A, AS	6 clocks
	HP 1662A, AS	4 clocks
	HP 1663A, AS	2 clocks
	HP 1664A	2 clocks

Clocks can be used by either one or two state analyzers at any time, except for the 1663A, 1663AS, and 1664A models, which can have only one state or timing analyzer. Clock edges can be ORed together and operate in single phase, two-phase demultiplexing, or two-phase mixed mode. Clock edge is selectable as positive, negative, or both edges for each clock.

State Clock Qualifier	The high or low of up to 4 of the 6 clocks can be ANDed or ORed with the clock specification.

Setup/Hold* [2]	
one clock, one edge	3.5/0 ns to 0/3.5 ns (in 0.5 ns increments)
one clock, both edges	4.0/0 ns to 0/4.0 ns (in 0.5 ns increments)
multi-clock, multi-edge	4.5/0 ns to 0/4.5 ns (in 0.5 ns increments)
Minimum State Clock Pulse Width* [2]	3.5 ns
Minimum Master to Master Clock Time* [2]	10.0 ns
Minimum Slave to Slave Clock Time [2]	10.0 ns
Minimum Master to Slave Clock Time [2]	0.0 ns

[1] Time may vary depending upon the mode of logic analyzer operation.

* Warranted Specification

Minimum Slave to Master Clock Time [2]	4.0 ns
Clock Qualifiers Setup/Hold [3]	4.0/0 ns (fixed)
State Tagging [3]	Counts the number of qualified states between each stored state. Measurement can be shown relative to the previous state or relative to trigger. Max. count is 4.29×10^9.
State Tag Count	0 to 4.29×10^9 (± 0 counts)
State Tag Resolution	1 count
Time Tagging [3]	Measures the time between stored states, relative to either the previous state or to the trigger. Max. time between states is 34.4 sec. Min. time between states is 8 ns.
Time Tag Count	8 ns to 34.4 seconds ± (8 ns + 0.01% of time tag value)
Time Tag Resolution	8 ns or 0.1% (whichever is greater)

Timing Analysis

Conventional Timing	Data stored at selected sample rate across all timing channels.	
Maximum Timing Speed [1]	250 MHz / 500 MHz	
Channel Count [1]	HP 1660A, AS	136/68
	HP 1661A, AS	102/51
	HP 1662A, AS	68/34
	HP 1663A, AS	34/17
	HP 1664A	34/17
Sample Period [1]	4 ns/2 ns minimum, 8.38 ms maximum	
Memory Depth per Channel [1]	4096/8192 samples	
Time Covered by Data [1]	Sample period × memory depth 16.3 µs min, 34.3 sec/68.6 sec max	
Transitional Timing	Sample is stored in acquisition memory only when the data changes. A time tag stored with each sample allows reconstruction of waveform display. Time covered by a full memory acquisition varies with the number of pattern changes in the data.	
Maximum Timing Speed [1]	125 MHz/250 MHz	
Channel Count [1]	HP 1660A, AS	136/68
	HP 1661A, AS	102/51
	HP 1662A, AS	68/34
	HP 1663A, AS	34/17
	HP 1664A	34/17
Sample Period [1]	8 ns/4 ns	
Time Covered by Data [1]	16.3 µs minimum, 9.7 hrs./6.5 hrs. maximum	
Maximum Time Between Transitions	34.3 s	
Number of Captured Transitions [1]	1023-2047/682-4094 Depending on input signals	
Glitch Capture Mode	Data sample and glitch information is stored every sample period	
Maximum Timing Speed	125 MHz	
Channel Count	HP 1660A, AS	68
	HP 1661A, AS	51
	HP 1662A, AS	34
	HP 1663A, AS	17
	HP 1664A	17
Sample Period	8 ns minimum, 8.38 ms maximum	
Minimum Glitch Width*	3.5 ns	
Maximum Glitch Width	Sample Period – 1 ns	
Memory Depth per Channel	2048 samples	
Time Covered by Data	Sample Period × 2048: 16.3 µs minimum, 17.1 sec maximum	

Time Interval Accuracy

Sample Period Accuracy	± 0.01%
Channel-to-Channel Skew	2 ns typical, 3 ns maximum
Time Interval Accuracy	± (Sample Period + channel-to-channel skew + 0.01% of time interval reading)
Maximum Delay After Triggering	Sample Period 2-8 ns : 8.389 ms Sample Period > 8 ns: 1,048,575 × sample period

Trigger Specifications

Trigger Macros	Trigger setups can be selected from a categorized list of trigger macros. Each macro is shown in graphical form and has a written description. Macros can be chained together to create a custom trigger sequence.	
Pattern Recognizers	Each recognizer is the AND combination of bit (0,1, or X) patterns in each label.	
Pattern Recognizers	10	
Pattern Width (in channels)	HP 1660A, AS	136
	HP 1661A, AS	102
	HP 1662A, AS	68
	HP 1663A, AS	34
	HP 1664A	34
Minimum Pattern and Range Recognizer Pulse Width	250 MHz and 500 MHz Timing Modes: 13 ns + channel-to-channel skew ≤ 125 MHz Timing Modes : 1 sample period + 1 ns + channel-to-channel skew + 0.01%	
Range Recognizers	Recognize data which is numerically between or on two specified patterns (ANDed combination of zeros and/or ones).	
Range Recognizers	2	
Range Width	32 channels	

Edge/Glitch Recognizers	Trigger on glitch or edge on any channel. Edge can be specified as rising, falling or either.
Edge/Glitch Recognizers	2 (in timing mode only)
Edge/Glitch Width (in channels)	HP 1660A, AS 136 HP 1661A, AS 102 HP 1662A, AS 68 HP 1663A, AS 34 HP 1664A 34
Edge/Glitch Recovery Time	Sample Period 2-8 ns: 28 ns Sample Period > 8 ns: 20 ns + sample period
Greater than Duration (timing only)	Sample period 2-8 ns: 8 ns to 8.389 ms. Accuracy is –2 ns to +10 ns Sample period > 8 ns (1 to 2 × 10^20) × sample period. Accuracy is –2 ns + sample period + 2 ns ± 0.01%
Less than Duration (timing only)	Sample period 2-8 ns: 8 ns to 8.389 ms. Accuracy is –2 ns to +10 ns. Sample period > 8 ns: (1 to 2×10^20) × sample period. Accuracy is 2 ns + sample period – 2 ns ± 0.01%
Qualifier	A user-specified term that can be any state, no state, any recognizer, (pattern, ranges or edge/glitch), any timer, or the logical combination (NOT, AND, NAND, OR, NOR, XOR, NXOR) of the recognizers and timers.
Branching	Each sequence level has a branching qualifier. When satisfied, the analyzer will branch to the sequence level specified.
Occurrence Counters	Sequence qualifier may be specified to occur up to 1,048,575 times before advancing to the next level. Each sequence level has its own counter.
Maximum Occurrence Count	1,048,575
Storage Qualification (state only)	Each sequence level has a storage qualifier that specifies the states that are to be stored.
Maximum Sequencer Speed	125 MHz
State Sequence Levels	12
Timing Sequence Levels	10
Timers	Timers may be Started, Paused, or Continued at entry into any sequence level after the first.
Timers	2
Timer Range	400 ns to 500 seconds
Timer Resolution	16 ns or 0.1% whichever is greater
Timer Accuracy	± 32 ns or ± 0.1%, whichever is greater
Timer Recovery Time	70 ns
Data In to Trigger Out BNC Port	110 ns typical

Acquisition, Measurement and Display Functions

Arming	Each analyzer can be armed by the Run key, the other analyzer, the oscilloscope (AS models only), or the Port In.
Run	Starts acquisition of data in specified trace mode.
Stop	In single trace mode or the first run of a repetitive acquisition, Stop halts acquisition and displays the current acquisition data. For subsequent runs in repetitive mode, Stop halts acquisition of data and does not change current display.
Trace Mode	Single mode acquires data once per trace specification; repetitive mode repeats single mode acquisitions until Stop is pressed or until pattern time interval or compare stop criteria are met.
Trigger	Displayed as a vertical dashed line in the timing waveform, state waveform and X-Y chart displays and as line 0 in the state listing and state compare displays.
Activity Indicators	Provided in the Configuration, State Format, and Timing Format menus for monitoring device-under-test activity while setting up the analyzer.
Labels	Channels may be grouped together and given a 6-character name called a *label*. Up to 126 labels in each analyzer may be assigned with up to 32 channels per label. Trigger terms may be given an 8-character name.

Measurement Functions

Markers	Two markers (x and o) are shown as dashed lines in the display.
Time Intervals	The x and o markers measure the time interval between events occurring on one or more waveforms or states (only available when time tagging is on).
Delta States	The x and o markers measure the number of tagged states between any two states.
Patterns	The x or o marker can be used to locate the nth occurrence of a specified pattern before or after trigger, or after the beginning of data. The o marker can also find the nth occurrence of a pattern before or after the x marker.

Statistics	x to o marker statistics are calculated for repetitive acquisitions. Patterns must be specified for both markers, and statistics are kept only when both patterns can be found in an acquisition. Statistics are minimum x to o time, maximum x to o time, average x to o time, and ratio of valid runs to total runs.
Compare Mode Functions	Performs post-processing bit-by-bit comparison of the acquired state data and Compare Image data.
Compare Image	Created by copying a state acquisition into the compare image buffer. Allows editing of any bit in the Compare Image to a 1, x or o.
Compare Image Boundaries	Each channel (column) in the compare image can be enabled or disabled via bit masks in the Compare Image. Upper and lower ranges of states (rows) in the compare image can be specified. Any data bits that do not fall within the enabled channels and the specified range are not compared.
Stop Measurement	Repetitive acquisitions may be halted when the comparison between the current state acquisition and the current Compare Image is equal or not equal.
Compare Mode Displays	Compare Listing display shows the Compare Image and bit masks; Difference Listing display highlights differences between the current state acquisition and the Compare Image.

Data Entry/Display

Display Modes	State Listing, State Waveforms, State Chart, State Compare Listing, Compare Difference Listing, Timing Waveforms, Timing Listing, interleaved time-correlated listing of two state analyzers (time tags on), and time-correlated State Listing with Timing Waveforms on the same display.
State X-Y Chart Display	Plots value of a specified label (on y-axis) versus states or another label (on x-axis). Both axes can be scaled.
Markers	Correlated to State Listing, State Compare, and State Waveform displays. Available as pattern, time, or statistics (with time counting) and states (with state counting on).
Accumulate	Chart display is not erased between successive acquisitions.
State Waveform Display	Displays state acquisitions in waveform format.
States/division	1 to 1000 states.
Delay	– 8191 to + 8192 states.
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
Timing Waveform Display	Displays timing acquisition in waveform format.
Sec/div	1 ns to 1000 s; 0.01% resolution.
Delay	– 2,500 s to + 2,500 s
Accumulate	Waveform display is not erased between successive acquisitions.
Overlay Mode	Multiple channels can be displayed on one waveform display line. When waveform size set to large, the value represented by each waveform is displayed inside the waveform in the selected base.
Displayed Waveforms	24 lines maximum on one screen. Up to 96 lines may be specified and scrolled through.
Bases	Binary, Octal, Decimal, Hexadecimal, ASCII (display only), User-defined symbols, two's compliment.
Symbols	
Pattern Symbols	User can define a mnemonic for the specific bit pattern of a label. When data display is SYMBOL, mnemonic is displayed where the bit pattern occurs.
Range Symbols	User can define a mnemonic covering a range of values. When data display is SYMBOL, values within the specified range are displayed as mnemonic + offset from base of range.
Number of Symbols	1000 maximum.

[1] Full Channel /Half Channel Modes

[2] Specified for an input signal VH= – 0.9V, VL = – 1.7V, slew rate = 1V/ns, and threshold = –1.3V

[3] Time or-state-tagging (Count Time or Count State) is available in the full-channel state mode. There is no speed penalty for tag use. Memory is halved when time or state tags are used unless a pod pair (34-channel group) remains unassigned in the Configuration menu.

HP 1660-Series Oscilloscope Specifications and Characteristics

General Information

Model Numbers	HP 1660AS, 1661AS, 1662AS, 1663AS
Number of Channels	2
Maximum Sample Rate	1 GSa/s per channel
Bandwidth [1] [5]	dc to 250 MHz (real time, dc coupled)
Rise Time [2] [5]	1.4 ns
Vertical Resolution	8 bits
Memory Depth	8k samples

Oscilloscope Probing

Input Coupling	1 MΩ: ac,dc 50 Ω: dc only
Input R [5]	1MΩ ± 1% 50Ω ± 1%
Input C	~ 7pF
Probes Included	Two HP 10430A probes; 10:1, 1 MΩ 6.5 pF

Vertical (at BNC)

Maximum Safe Input Voltage	1 MΩ : ±250 V 50 Ω : 5 V rms
Vertical Sensitivity Range (1:1 Probe)	1 MΩ: ±250 V (ac + dc, <10 kHz) 50 Ω: 5 V rms
Probe Factors	Any integer ratio from 1:1 to 1000:1
Vertical (dc) Gain Accuracy [3]	± 1.25% of full scale
dc Offset Range (1:1 probe)	± 2V to ± 250V (depending on the vertical sensitivity)
dc Offset Accuracy [5]	± [1.0% of channel offset + 2.0% of full scale]
Voltage Measurement Accuracy [5]	± [1.25% of full scale + offset accuracy + 0.016 V/div]
Channel-to-Channel Isolation	dc to 50 MHz – 40 dB 50 MHz to 250 MHz – 30 dB

Horizontal

Time Base Range	1 ns/div to 5 s/div
Time Base Resolution	20 ps ± [(0.005% of Δt) + ($2 \times 10^{-6} \times$ delay setting) + 150 ps]
Maximum Negative Acquisition Delay	– 4 µs to – 40 s (depending on the sample rate)
Maximum Positive Acquisition Delay	16.7 ms to 2.5 ks (depending on sample rate)
Time Interval Measurement Accuracy [4] [5]	± [(0.005% of Δt) + ($2 \times 10^{-6} \times$ delay setting) + 150 ps]

Oscilloscope Triggering

Trigger Level Range	Bounded within channel display window
Trigger Sensitivity [5]	dc to 50 MHz: 0.063 × Full Scale 50 MHz to 250 MHz: 0.125 × Full Scale

Trigger Modes

Immediate	Triggers immediately after arming condition is met. (Arming condition is Run, Group Run, cross arming signal, or Port In BNC signal).
Edge	Triggers on rising or falling edge from channel 1 or 2.
Pattern	Triggers on entering or exiting logical pattern specified across channels 1 or 2. Each channel can be specified as high (H), low (L), or don't care (X) with respect to the level settings in the edge trigger menu. Patterns must be >1.75 ns in duration to be recognized.
Time-Qualified Pattern	Triggers on the exiting edge of a pattern which meets the user-specified duration criterion. Greater than, less than, or within range duration criterion can be used. Duration range is 20 ns to 160 ns. Recovery time after valid patterns with invalid duration is <12 ns.
Events Delay	Triggers on the nth edge or pattern as specified by the user. Time-qualification is applied only to the 1st of n patterns.
Auto-Trigger	Self-triggers if no trigger condition is found ~ 50 ms after arming.

Measurement Functions

Time Markers	Two markers (x and o) measure time intervals manually, or automatically with statistics.
Voltage Markers	Two markers (a and b) measure voltage and voltage differences.
Automatic Measurements	Period, frequency, rise time, fall time, +width, –width, peak-to-peak voltage, overshoot, and undershoot.

[1] Upper bandwidth reduces by 2.5 MHz for every degree C above 35°C.

[2] Rise time calculated as $t_r = \frac{0.35}{\text{bandwidth}}$

[3] Vertical gain accuracy decreases 0.08% per degree C from software calibration temperature.

[4] Specification applies at the maximum sampling rate. At lower rates, replace 150 ps in the formula with (0.15 × sample interval) where sample interval is defined as 1/sample rate.

[5] Specifications (valid within ± 10°C of auto-calibration temperature)

Ordering Information

HP 1660A
136-channel benchtop logic analyzer
HP 1660AS
136-channel analyzer with a built-in, 2-channel oscilloscope

HP 1661A
102-channel benchtop logic analyzer
HP 1661AS
102-channel analyzer with a built-in, 2-channel oscilloscope

HP 1662A
68-channel benchtop logic analyzer
HP 1662AS
68-channel analyzer with a built-in, 2 channel oscilloscope

HP 1663A
34-channel benchtop logic analyzer
HP 1663AS
34-channel analyzer with a built-in, 2-channel oscilloscope

HP 1664A
Value-priced 34-channel benchtop logic analyzer
Option 020*
RS-232 and HP-IB interfaces with programming manual
Option 0B5*
Quick-Start Training Kit

Option 0B3
Service Manual
Option 908 or 1CM
Rackmount Kit
Option UK9
Front panel cover
Option W30
Three-year extended repair service

HP E2427A
HIL Keyboard for logic analyzers
HP E2460AS, E2460B, E2461B and E2462B
Hewlett-Packard-installed upgrade kits (add an oscilloscope or more channels to selected models)

HP 1180B Testmobile
HP 35183A Work Surface
Attaches to HP 1180B Testmobile as a platform for mouse operation

** This option is standard equipment on all models except the HP 1664A.*

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below for the location of your nearest sales office.

United States:
Hewlett-Packard Company
Test and Measurement Organization
5301 Stevens Creek Blvd.
Bldg. 51L-SC
Santa Clara, CA 95052-8059
1 800 452 4844

Canada:
Hewlett-Packard Canada Ltd.
5150 Spectrum Way
Mississauga, Ontario
L4W 5G1
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1180 AZ Amstelveen
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